

AM62A STARTER KIT EVM

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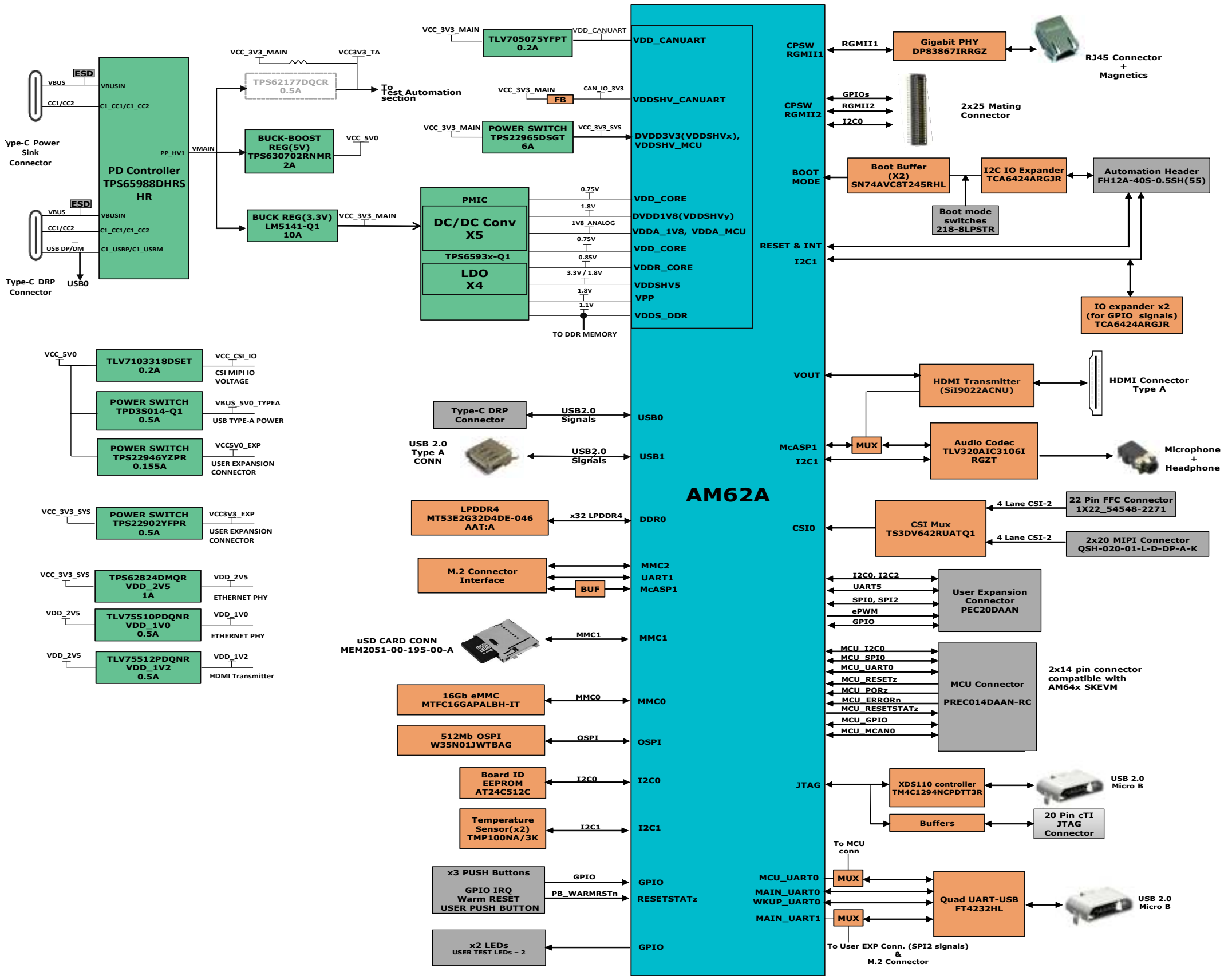
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REV	E2
VER	2.0

REVISION HISTORY

E1	VER #	DATE	DESCRIPTION OF CHANGES	AUTHOR	REVIEWED BY	APPROVED BY
	0.01	21 MARCH 2022	Initial Draft	Mistral Design Team		
	0.02	30 MARCH 2022	Updated CSI , LPDDR4 & PD CONTROLLER SECTION	Mistral Design Team		
	0.03	14 APR 2022	Updated PMIC section	Mistral Design Team		
	0.04	02 MAY 2022	Updated Internal Review comments	Mistral Design Team		
	0.05	04 MAY 2022	Updated SoC Decaps & CSI FET connections for routing ease	Mistral Design Team		
	0.06	09 MAY 2022	Updated PMIC section	Mistral Design Team		
	0.07	10 MAY 2022	Net swapping in OSPI and HDMI groups of signals	Mistral Design Team		
	0.08	11 MAY 2022	Updated Power supply-2 (VCC_3V3_MAIN) section with new regulator, replaced RGMII2 PHY section for accomodating ethernet ADD-ON boards(Industrial and Automotive PHY based)	Mistral Design Team		
	0.09	12 MAY 2022	Added Matting Connectors for ADD-ON boards and main board Updated power achitecture and I2C tree digrams	Mistral Design Team		
	0.10	12 MAY 2022	Added Matting Connectors for ADD-ON boards and main board	Mistral Design Team		
	0.11	13 MAY 2022	Added 3T caps for VDD_LPDDR4 SOC power rail	Mistral Design Team		
	0.12	16 MAY 2022	TI Review Comments implemented	Mistral Design Team		
	0.13	18 MAY 2022	Updated single port PD controller to Dual PD to match software requirements	Mistral Design Team		
	0.14	19 MAY 2022	Separated RGMII Add On Boards to individual schematics	Mistral Design Team		
	0.15	24 MAY 2022	Updated PMIC GPIO connections as per TI review comments	Mistral Design Team		
	0.16	27 MAY 2022	TI Review Comments implemented	Mistral Design Team		
	0.17	30 MAY 2022	Updated M.2 connector section Added I2C signals for RGMII Add-On connector Added LDO for VDD_CANUART signals Part References Back annotated from PCB file	Mistral Design Team		
	0.18	31 MAY 2022	Updated to SOC I2C0 for RGMII board detect Removed ground connection from M.2 screw	Mistral Design Team		
	0.19	1 JUNE 2022	Modified MCU User Interrupt signals Updated TI review comments	Mistral Design Team		
E2	0.20	15 JUNE 2022	CSI MIPI Connector (J1) marked as present as per TI Comments	Mistral Design Team		
	1.0	17 JUNE 2022	Baselined	Mistral Design Team		
	1.01	19 SEPT 2022	Updated design with changes mentioned in "AM62A_SKEVM_Change_List_For_REV_E2" document	Mistral Design Team		
	1.02	20 SEPT 2022	Replaced the INA filter resistors from existing 10E to 0E as per TI recommendations	Mistral Design Team		
	2.0	20 SEPT 2022	Baselined	Mistral Design Team		

BLOCK DIAGRAM AM62A-SKEVM



Designed for TI by Mistral Solutions Pvt Ltd



Title BLOCK DIAGRAM AM62A_SKEVM

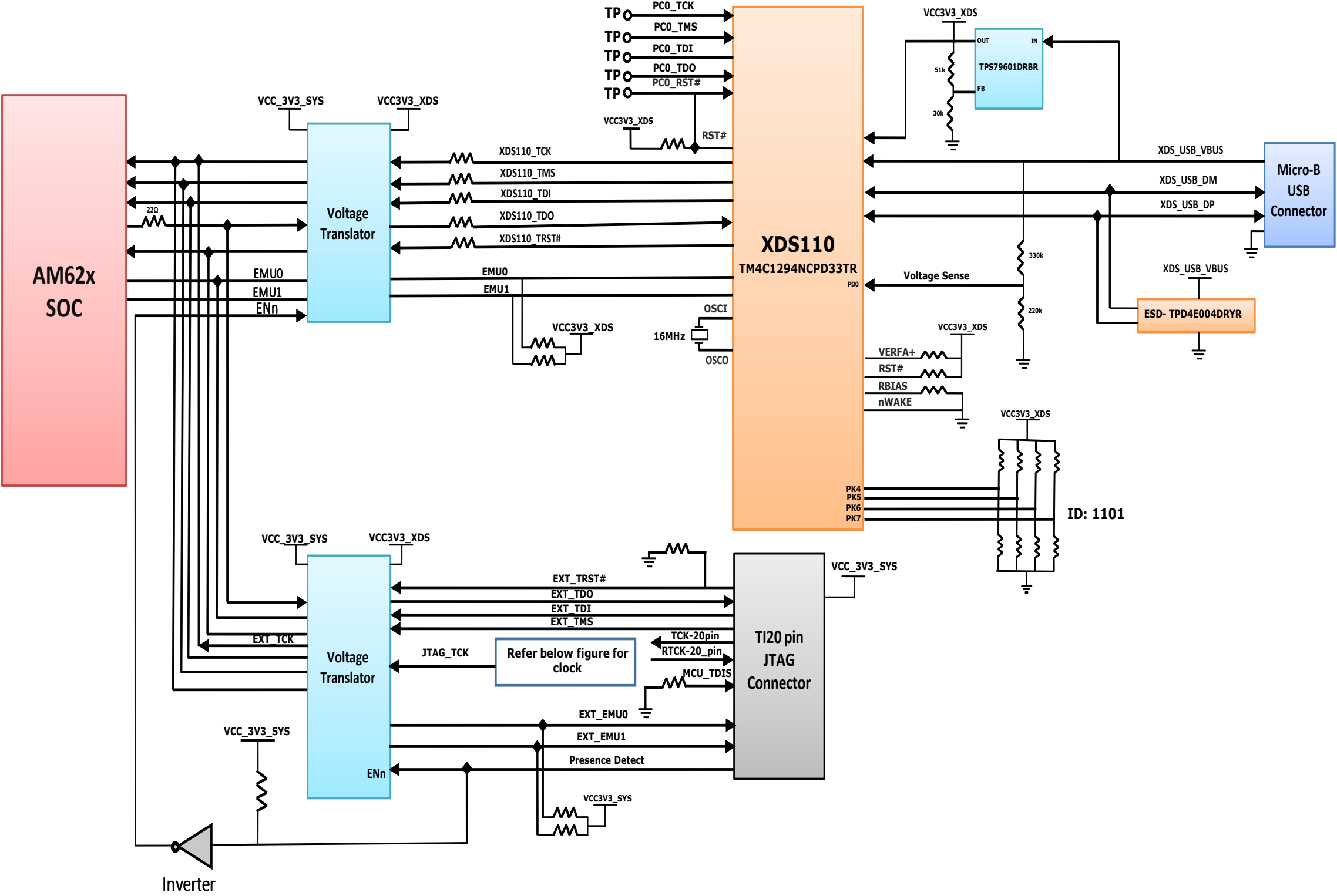
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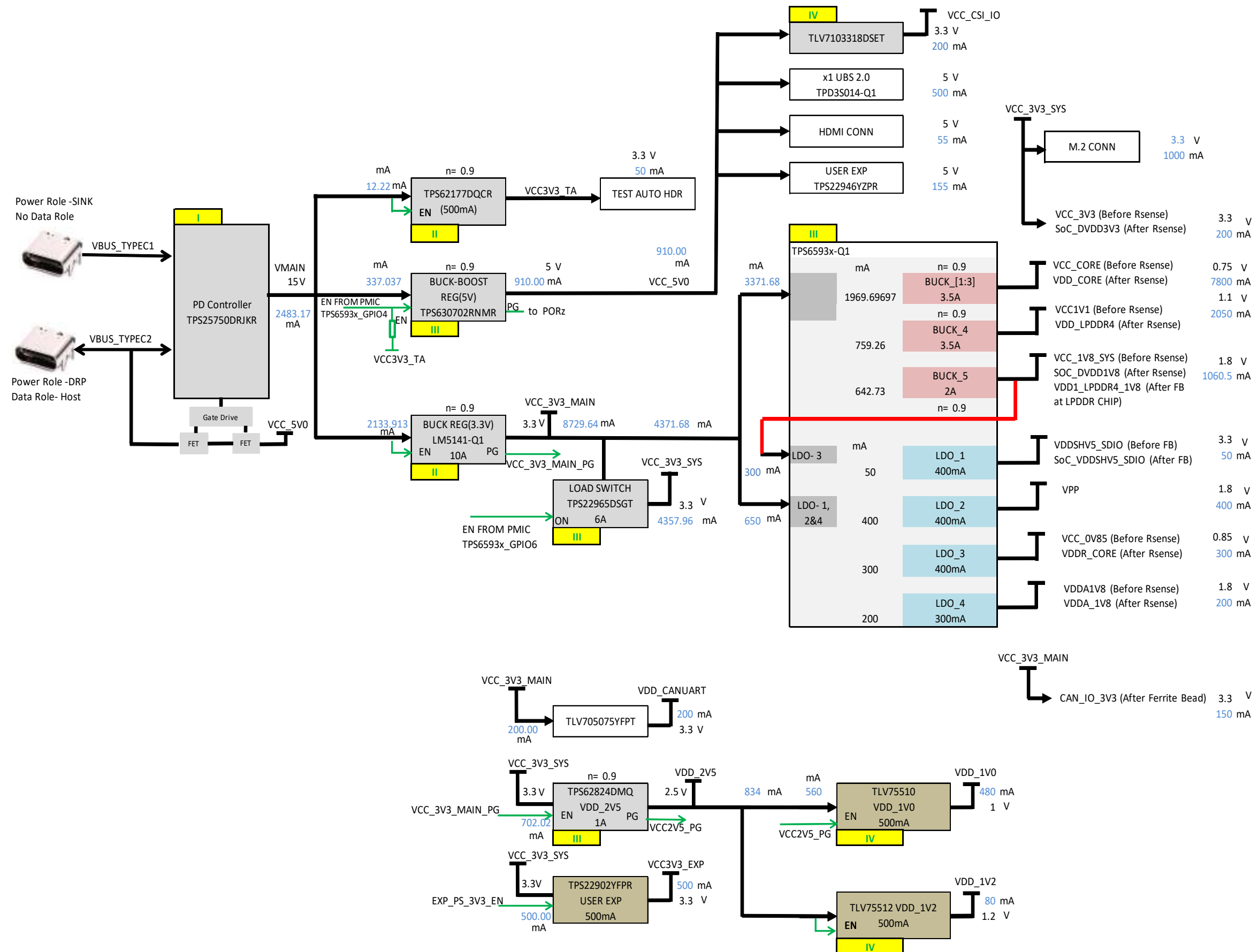
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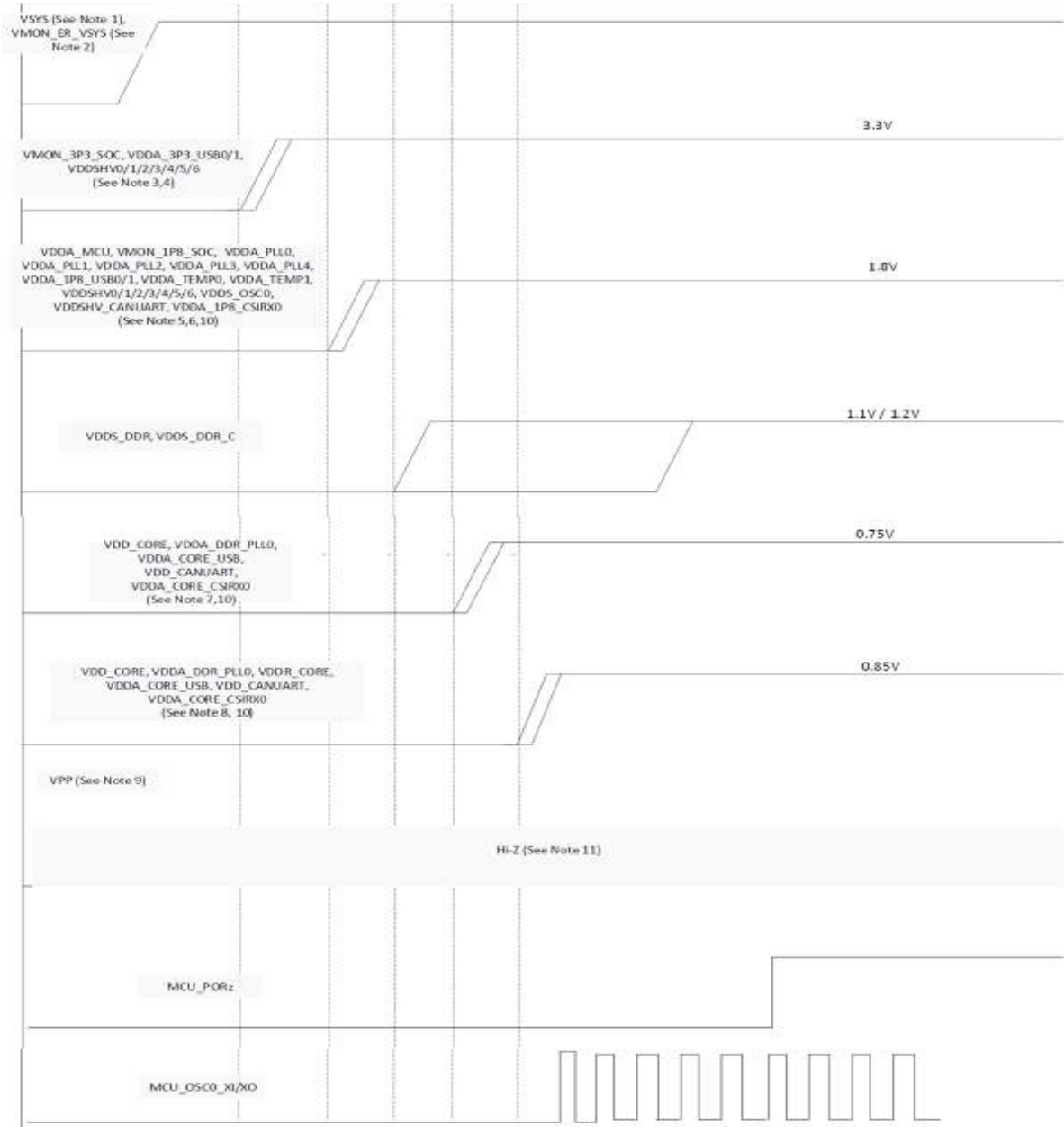
BLOCK DIAGRAM_XDS110



POWER BLOCK DGM



POWER SEQUENCE



Notes:

1. VSYS represents the name of a supply which sources power to the entire system. This supply is expected to be a pre-regulated supply that sources power management devices which source all other supplies.
2. VMON_ER_VSYS input is used to monitor VSYS via an external resistor divider circuit. For more information, see Section 7.3.4, System Power Supply Monitor Design Guidelines.
3. VDDSHV_MCU and VDDSHVx [x=0-6] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. When any of the VDDSHV_MCU or VDDSHVx [x=0-6] IO supplies are operating at 3.3V, they shall be ramped up with other 3.3V supplies during the 3.3V ramp period defined by this waveform.
4. The VMON_3P3_SOC input is used to monitor supply voltage and shall be connected to the respective 3.3V supply source.
5. VDDSHV_MCU and VDDSHVx [x=0-6] are dual voltage IO supplies which can be operated at 1.8V or 3.3V depending on the application requirements. When any of the VDDSHV_MCU or VDDSHVx [x=0-6] IO supplies are operating at 1.8V, they shall be ramped up with other 1.8V supplies during the 1.8V ramp period defined by this waveform.
6. The VMON_IP8_SOC input is used to monitor supply voltage and shall be connected to the respective 1.8V supply source.
7. VDD_CORE, VDDA_DDR_PLL0, VDD_CANUART, VDDA_CORE_USB, and VDDA_CORE_CSIRX0 can be operate at 0.75V or 0.85V. When VDD_CORE is operating at 0.75V then VDDA_DDR_PLL0, VDD_CANUART, VDDA_CORE_USB0/1, and VDDA_CORE_CSIRX0 shall also operate 0.75V and shall be ramped up prior to all 0.85V supplies as shown in this waveform.
8. VDD_CORE, VDDA_DDR_PLL0, VDD_CANUART, VDDA_CORE_USB, and VDDA_CORE_CSIRX0 can be operated at 0.75V or 0.85V. When VDD_CORE is operating at 0.85V then VDDA_DDR_PLL0, VDD_CANUART, VDDA_CORE_USB, and VDDA_CORE_CSIRX0 shall also operate at 0.85V and shall be ramped up with other 0.85V supplies during the 0.85V ramp period defined by this waveform.
9. VPP is the 1.8V eFuse programming supply, which shall be left floating (HiZ) or grounded during power-up/down sequences and during normal device operation. This supply shall only be sourced while programming eFuse.
10. VDDA_CORE_CSIRX0 and VDDA_IP8_CSIRX0 are analog supplies that for the CSI DPHY. If CSI is not used then these supplies may be shorted to ground.

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Title POWER SEQUENCE

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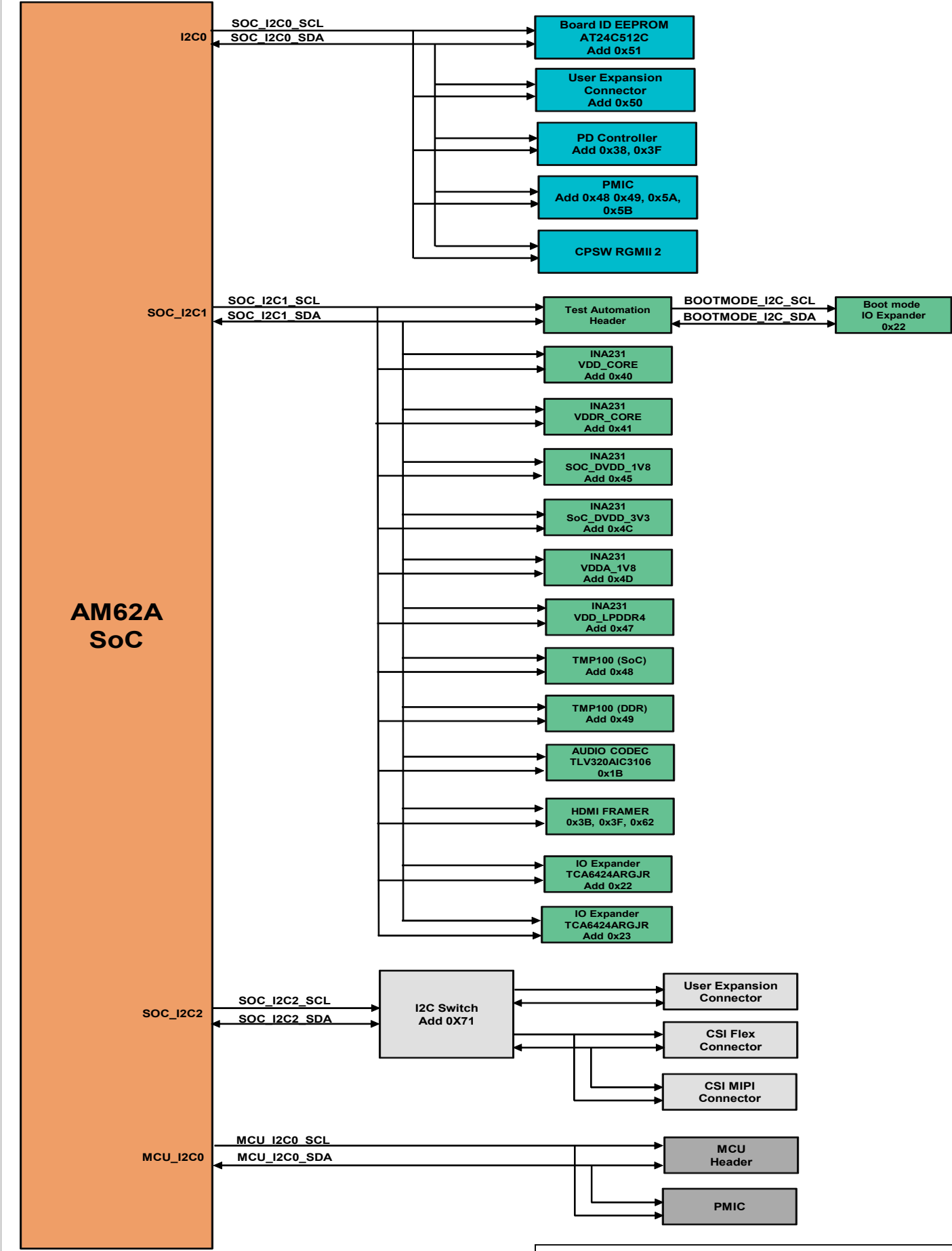
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I2C TREE



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Title I2C TREE		
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GPIO MAPPING TABLE

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	FUNCTIONALITY	GPIO USED	PACKAGE SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE RAIL CONNECTED ON SKEVM
1	Enable for WLAN Interface	WLAN_EN	ENABLE	GPIO0_71	MMC2_SD CD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	WLAN_IRQ	INTERRUPT	GPIO0_72	MMC2_SD WP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC	ENABLE	MCU_GPIO0_0	MCU_SPIO_CS0	OUTPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt	CPSW_RGMII_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	MCU Header GPIO0_16	MCU_GPIO0_16	GPIO	MCU_GPIO0_16	MCU_MCAN1_RX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
7	MCU Header GPIO0_15	MCU_GPIO0_15	GPIO	MCU_GPIO0_15	MCU_MCAN1_TX	NA	NA	NA	VDDSHV_CANUART	CAN_IO_3V3
8	PMIC Interrupt	PMIC_INT_B	INTERRUPT	GPIO0_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV3	SoC_DVDD3V3
9	CAN-FD fast wake up signal from switch	CAN_FD_WKUP_SW_INH	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	CAN_IO_3V3
10	CAN-FD fast wake signal from MCU header	CAN_FD_WKUP_HDR_INH								
11	Interrupt signal from Automotive Ethernet ADD-ON board	CPSW_ETH2_INH								
12	User test LED control signal	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SD WP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	Watchdog trigger input signal for Watchdog Trigger mode	PMIC_WDOG_TRIGG	ENABLE	MCU_GPIO0_19	WKUP_I2C0_SCL	INPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
14	WKUP Signal from RGMII2	CPSW_ETH2_WAKE	INTERRUPT	MCU_GPIO0_20	WKUP_I2C0_SDA	INPUT	LOW	HIGH	VDDSHV_MCU	SoC_DVDD3V3
15	User EXP Conn GPIO	EXP_GPIO1_22	GPIO	GPIO1_22	UART0_CTSn	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	IO Expander Interrupt	GPIO1_23_INTn	INTERRUPT	GPIO1_23	UART0_RTSn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
17	User Interrupt									
18	User EXP Conn GPIO	EXP_GPIO0_14_LT	GPIO	GPIO0_14	OSPI0_CSn3	NA	NA	NA	VDDSHV1	SoC_DVDD1V8
19	PMIC Standby Disable	PMIC_LPM_EN0	ENABLE	MCU_GPIO0_22	PMIC_LPM_EN0	OUTPUT	LOW	HIGH	VDDSHV_CANUART	CAN_IO_3V3
20	User EXP Conn GPIO	EXP_EHRPWM1_B	GPIO	GPIO1_10	MCASP0_AXR0	NA	NA	NA	VDDSHV0	SoC_DVDD3V3
IO EXPANDER - 01										
1	Ethernet Daughter Card plug in detect	RGMII2_BRD_CONN_DET	DETECTION	IO EXPANDER-P00		INPUT	HIGH	LOW		VCC_3V3_SYS
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER-P01		OUTPUT	HIGH	LOW		VCC_3V3_SYS
3	M.2 module Bluetooth LDO Enable	BT_EN_SOC	ENABLE	IO EXPANDER-P02		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER-P03		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_EN	ENABLE	IO EXPANDER-P04		OUTPUT	NA	HIGH		VCC_3V3_SYS
6	EXP CONN 3.3V Power Switch Enable	EXP_PS_3V3_EN	ENABLE	IO EXPANDER-P05		OUTPUT	LOW	HIGH		VCC_3V3_SYS
7	EXP CONN 5V Power Switch Enable	EXP_PS_5V0_EN	ENABLE	IO EXPANDER-P06		OUTPUT	LOW	HIGH		VCC_3V3_SYS
8	EXP CONN HAT Board Detection	EXP_HAT_DETECT	DETECTION	IO EXPANDER-P07		INPUT	HIGH	LOW		VCC_3V3_SYS
9	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	RESET	IO EXPANDER-P10		OUTPUT	HIGH	LOW		VCC_3V3_SYS
10	eMMC Reset control GPIO	GPIO_EMMC_RSTn	RESET	IO EXPANDER-P11		OUTPUT	HIGH	LOW		VCC_3V3_SYS
11	SOC UART1 Mux Select	UART1_FET_BUF_EN	ENABLE	IO EXPANDER-P12		OUTPUT	HIGH	LOW		VCC_3V3_SYS
12	BT UART WKUP Signal	BT_UART_WAKE_SOC_3V3	INTERRUPT	IO EXPANDER-P13		INPUT	HIGH	LOW		VCC_3V3_SYS
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER-P14		OUTPUT	HIGH	LOW		VCC_3V3_SYS
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO0	INPUT/OUTPUT	IO EXPANDER-P15		NA	NA	NA		VCC_3V3_SYS
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER-P16		NA	NA	NA		VCC_3V3_SYS
16	WLAN Alert Interrupt	WLAN_ALERTn	INTERRUPT	IO EXPANDER-P17		INPUT	HIGH	LOW		VCC_3V3_SYS
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER-P20		INPUT	HIGH	LOW		VCC_3V3_SYS
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO	IO EXPANDER-P21		NA	HIGH	NA		VCC_3V3_SYS
19	MCASP1 Enable and Direction Control	MCASP1_FET_EN	ENABLE	IO EXPANDER-P22		OUTPUT	LOW	LOW		VCC_3V3_SYS
20		MCASP1_BUF_BT_EN	ENABLE	IO EXPANDER-P23		OUTPUT	LOW	HIGH		VCC_3V3_SYS
21		MCASP1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P24		OUTPUT	HIGH	-		VCC_3V3_SYS
22		UART1_FET_SEL	DIRECTION CONTROL	IO EXPANDER-P25		OUTPUT	HIGH	-		VCC_3V3_SYS
23	Power Delivery I2C Interrupt Request	PD_I2C_IRQ	INTERRUPT	IO EXPANDER-P26		INPUT	HIGH	LOW		VCC_3V3_SYS
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER-P27		OUTPUT	LOW	HIGH		VCC_3V3_SYS
IO EXPANDER – 02										
1	SoC SPIO MUX Selection	SPIO_FET_SEL	CONTROL	IO EXPANDER-P20		OUTPUT	LOW	-		VCC_3V3_SYS
2	SoC SPIO MUX Enable	SPIO_FET_OE	ENABLE	IO EXPANDER-P21		OUTPUT	LOW	LOW		VCC_3V3_SYS
3	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER-P22		OUTPUT	HIGH	LOW		VCC_3V3_SYS
4	CSI flex and mipi MUX Selection	CSI_SEL2	CONTROL	IO EXPANDER-P23		OUTPUT	HIGH	-		VCC_3V3_SYS
5	CSI MUX Enable	CSI_EN	ENABLE	IO EXPANDER-P24		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
6	Auto PHY mode config	AUTO_100M_1000M_CONFIG	CONTROL	IO EXPANDER-P25		OUTPUT	NA	NA		VCC_3V3_SYS
7	CSI I/O Voltage Select(VCC_CSI_IO)	CSI_VLDO_SEL	CONTROL	IO EXPANDER-P26		OUTPUT	LOW	-		VCC_3V3_SYS
8	WLAN Reset control GPIO	SOC_WLAN_SDIO_RST	RESET	IO EXPANDER-P27		OUTPUT	HIGH	LOW		VCC_3V3_SYS
9	Wilink Enable	WL_LT_EN	ENABLE	IO EXPANDER-P10		OUTPUT	HIGH	HIGH		VCC_3V3_SYS
10	CSI Reset Control GPIO	CSI_RSTz	RESET	IO EXPANDER-P11		OUTPUT	LOW	LOW		VCC_3V3_SYS

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Title GPIO MAPPING TABLE

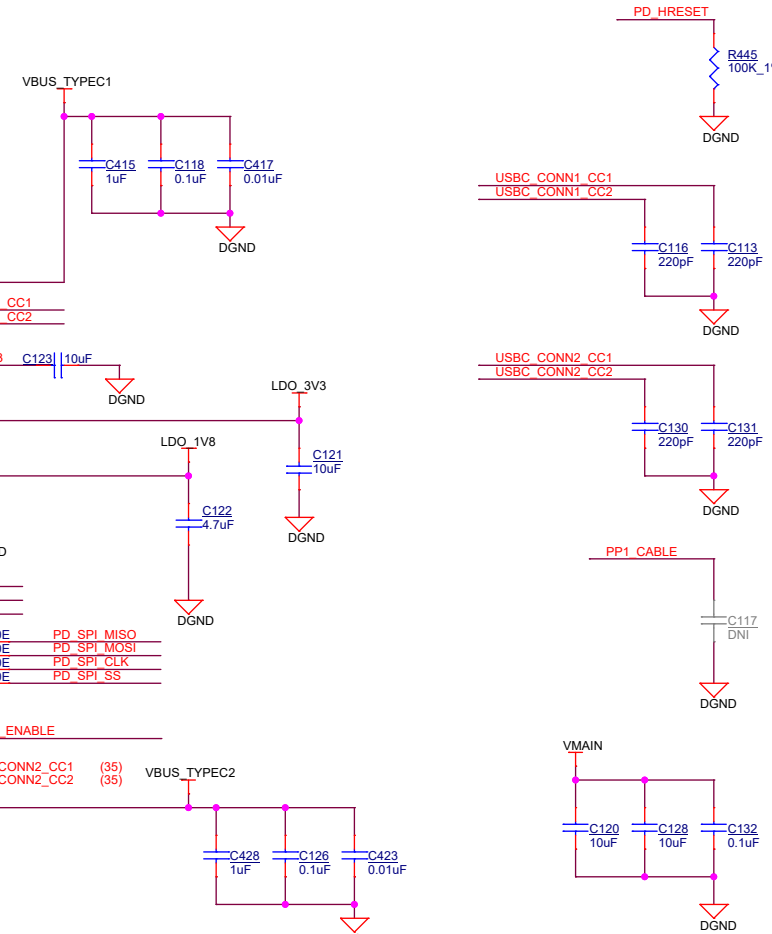
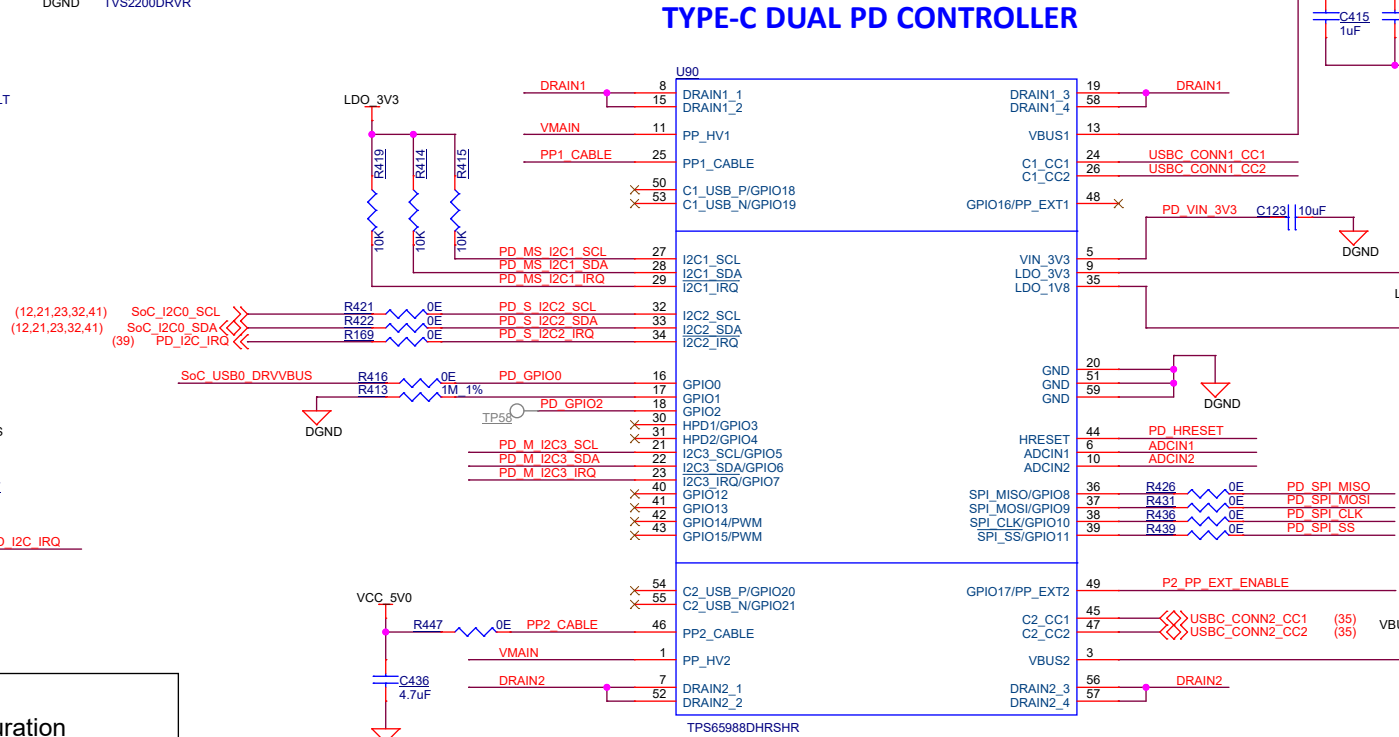
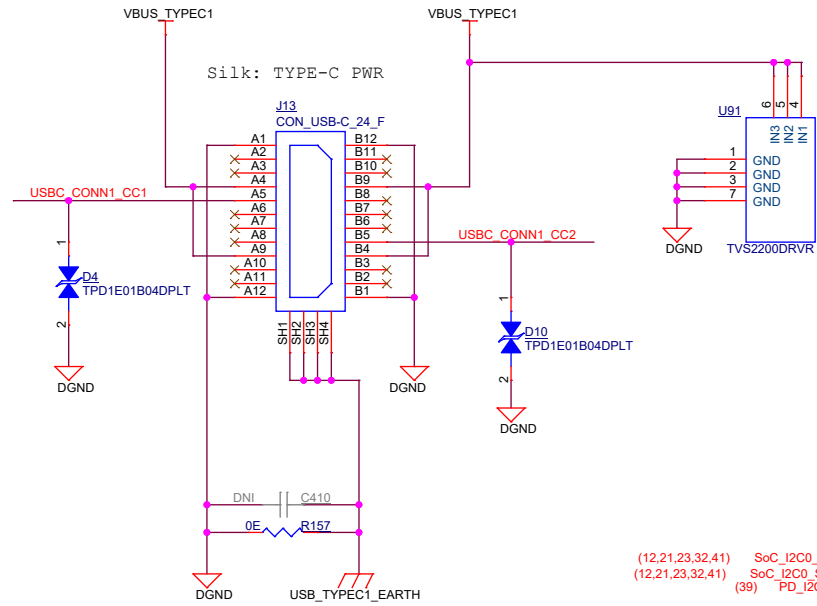
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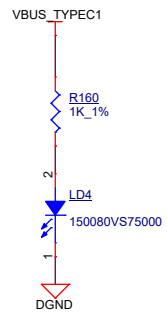
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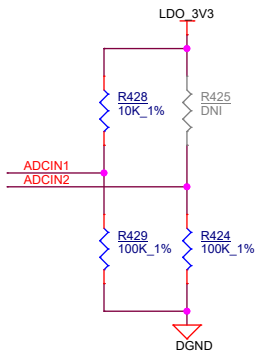
USB TYPE-C POWER



POWER INDICATION LED: VBUS_TYPEC1

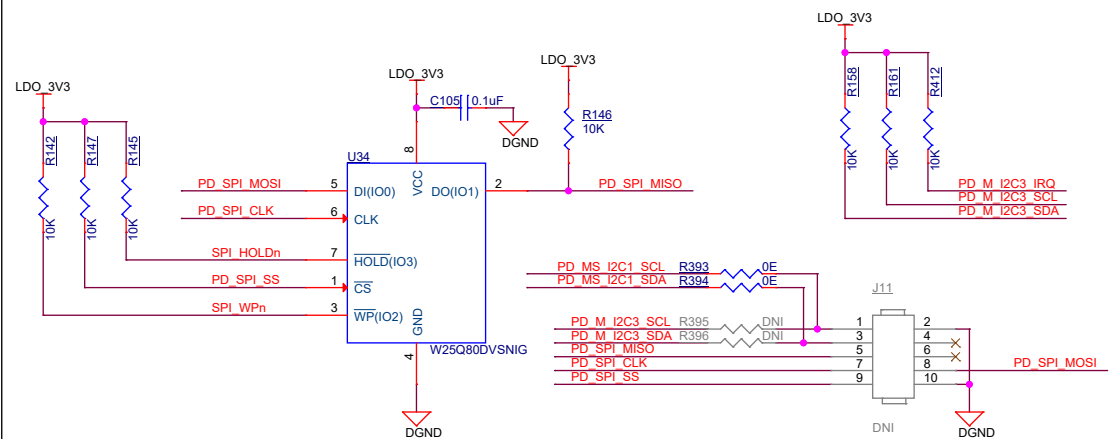


BP_NoWait
Safe Configuration

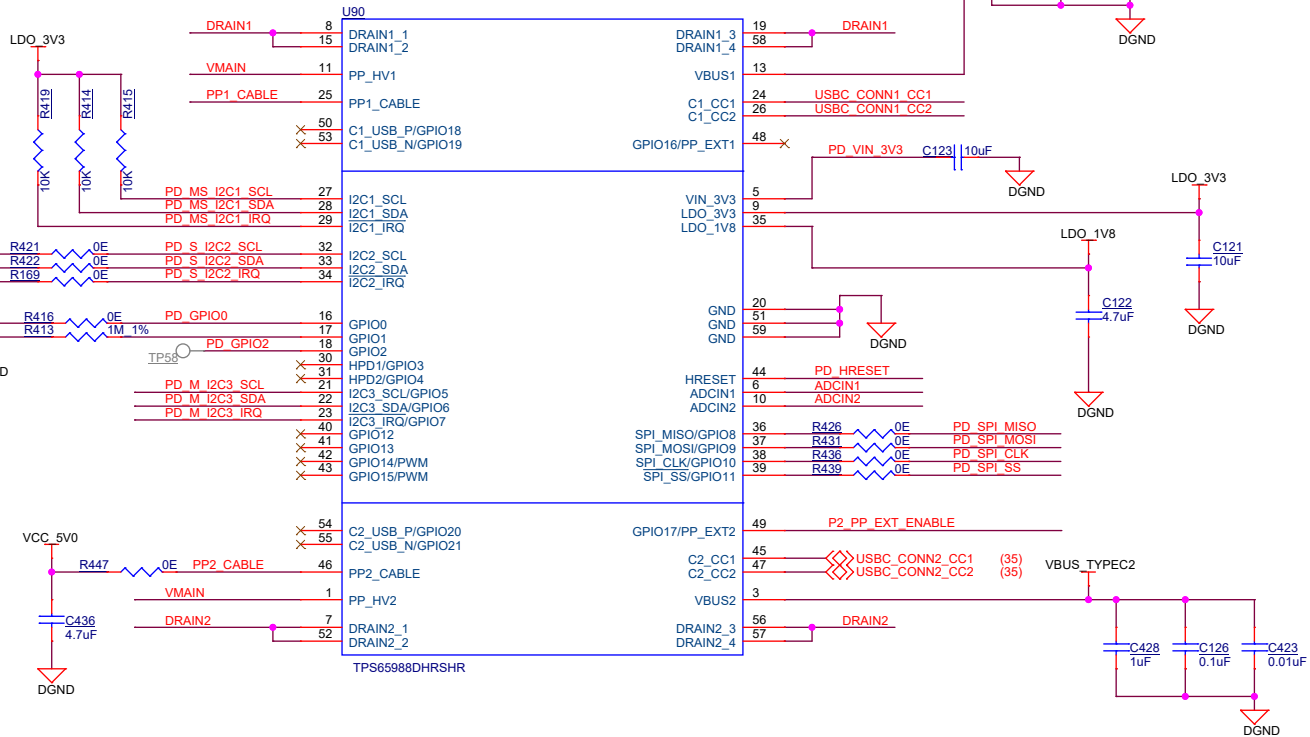


I2C Slave Address	Port1	Port2
I2C2(Default)	0x38	0x3F
I2C1	0x20	0x24

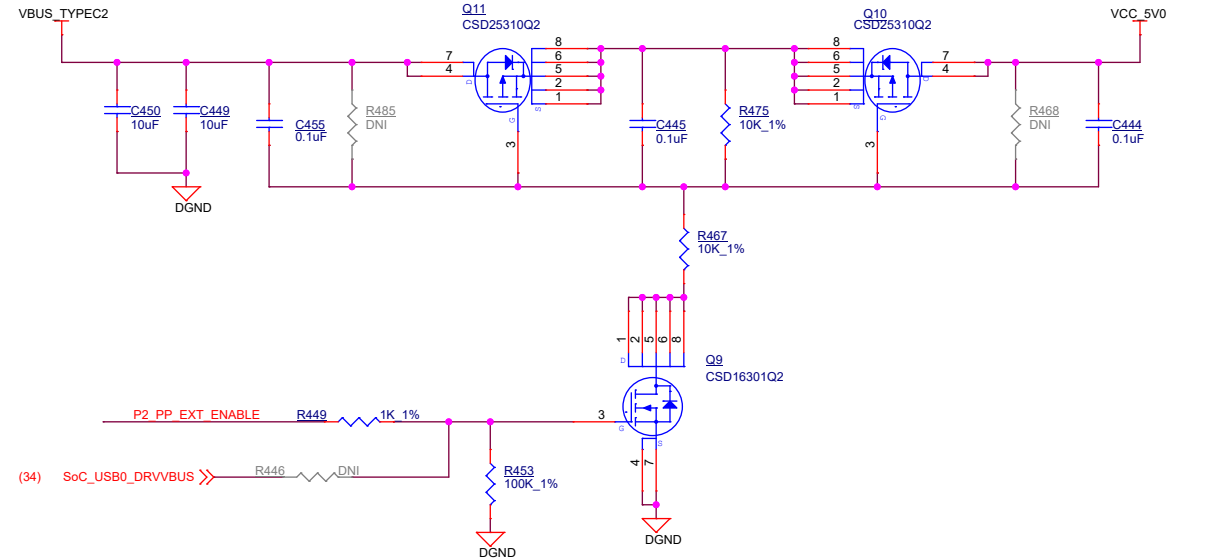
SPI EEPROM & PROGRAMMING HEADER



TYPE-C DUAL PD CONTROLLER



EXTERNAL POWER PATH FOR SOURCING, 5V/0.5A



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Title	USB TYPE-C
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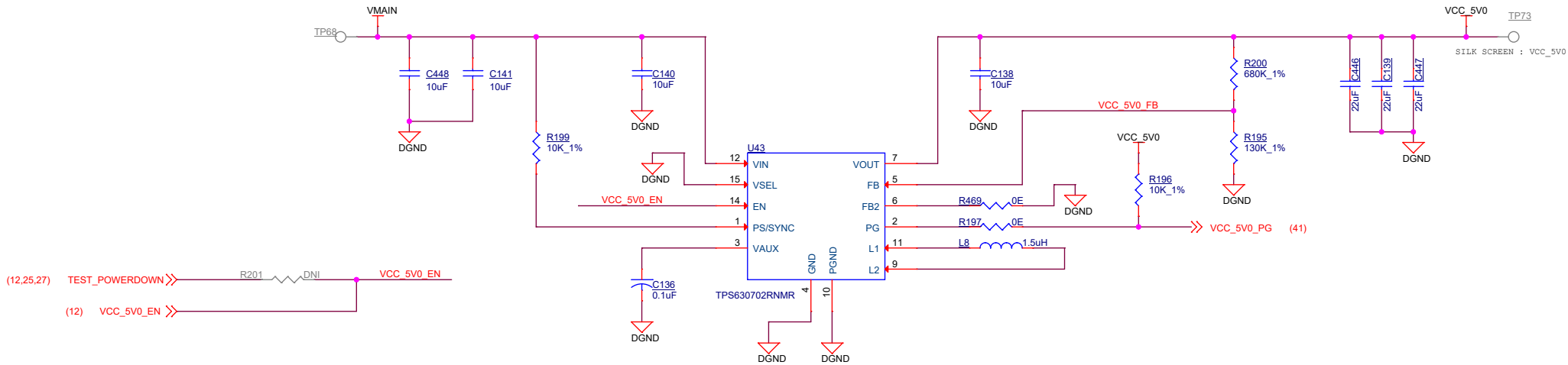
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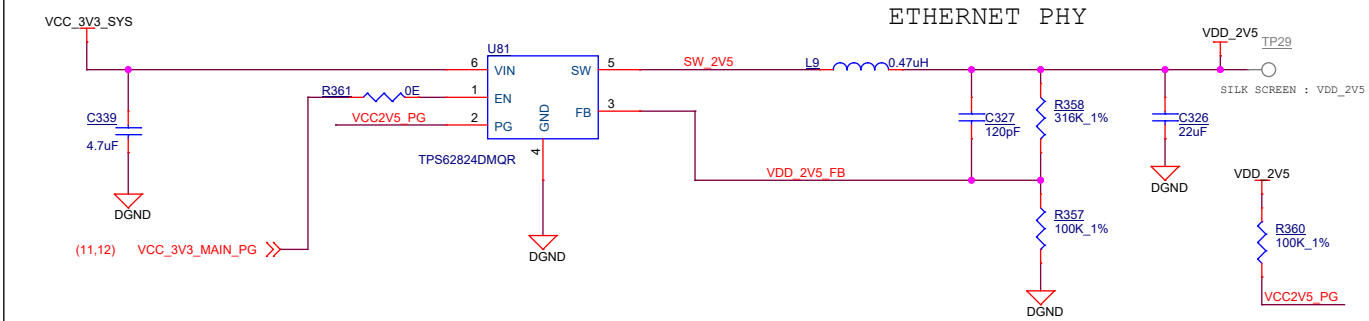
PERIPHERAL POWER SUPPLY-1

VinMin = 4.5V
VinMax = 15V
Vout = 5V @ 2A



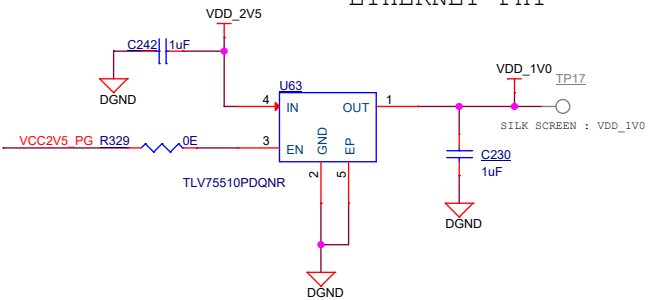
2.5V, 1.0AMPS SUPPLY

ETHERNET PHY

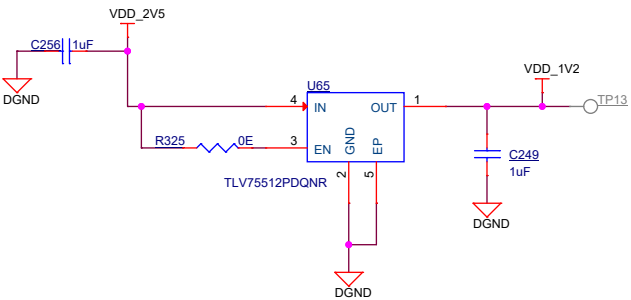


1.0V, 0.5AMPS SUPPLY

ETHERNET PHY



1.2V, 0.5AMPS SUPPLY



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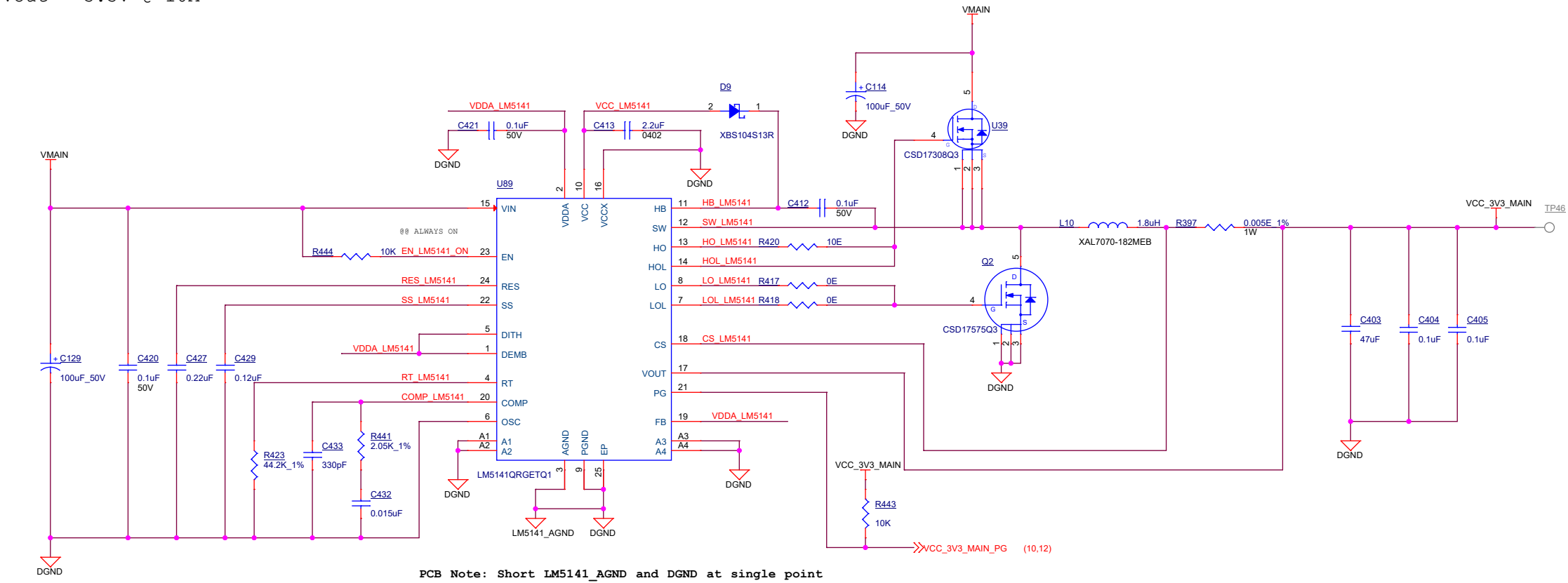
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PERIPHERAL POWER SUPPLY-2

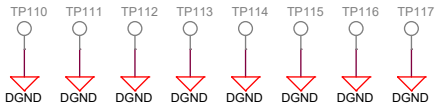
3.3V, 10.0 AMPS SUPPLY

VinMin = 4.5V
VinMax = 15V
Vout = 3.3V @ 10A



(33) ETH_CAN_INH_PREREG >> DNI R81 EN_LM5141_ON

GND TEST POINTS

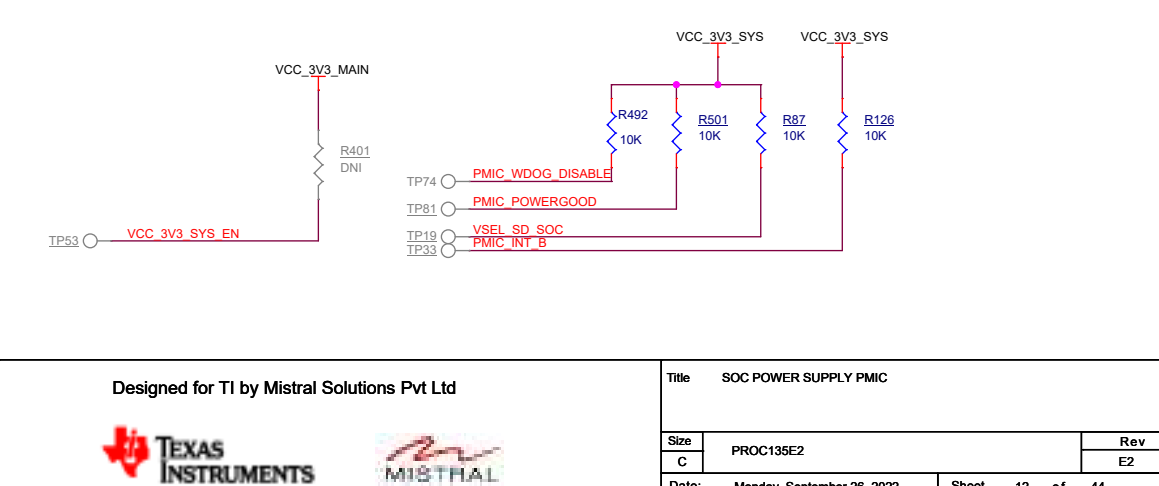
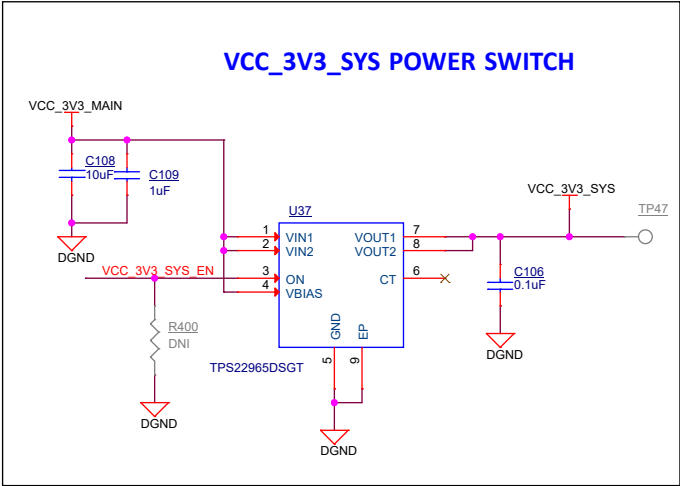
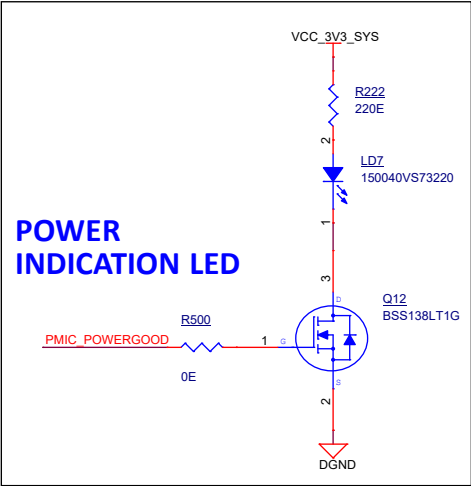
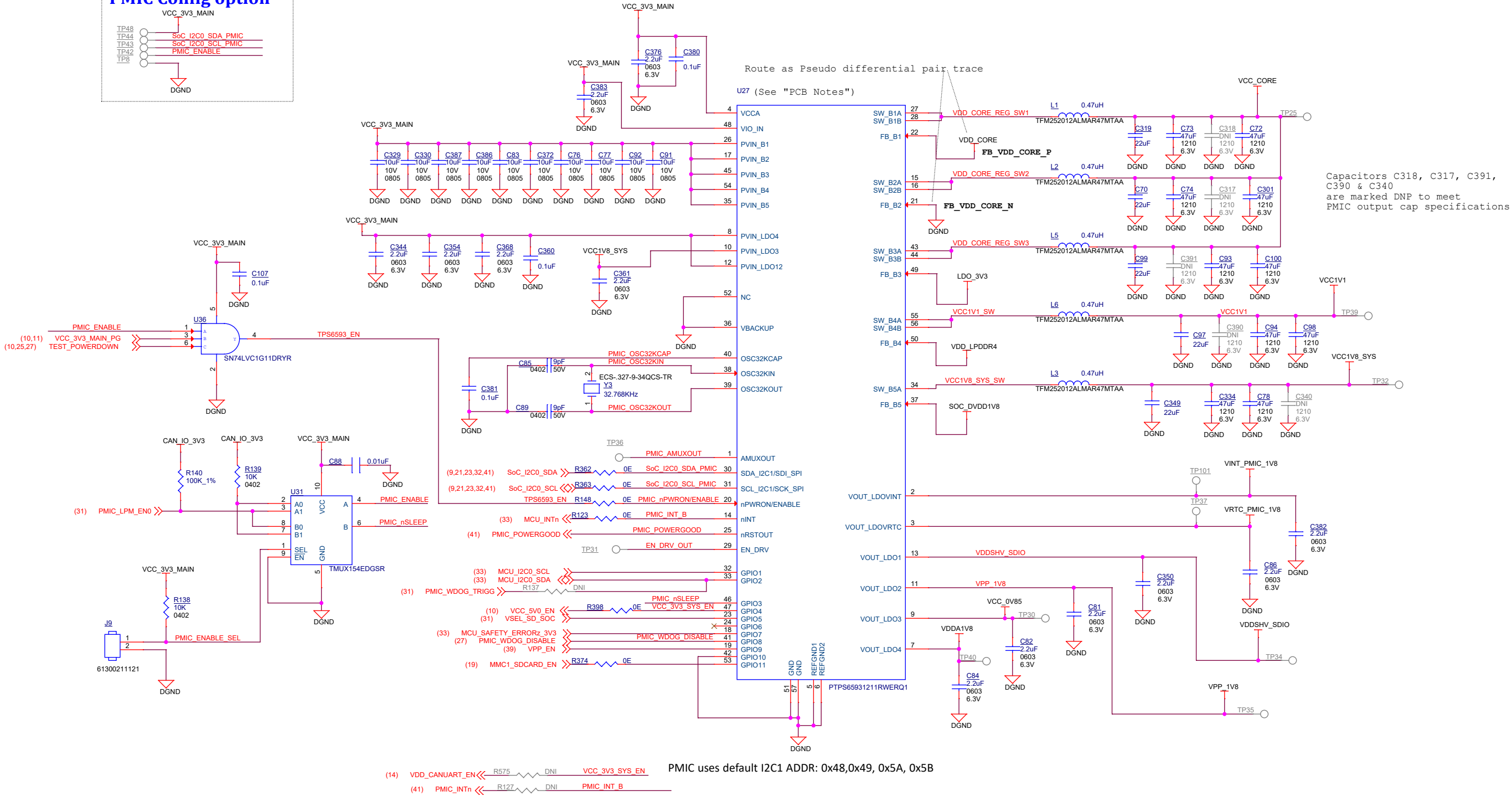
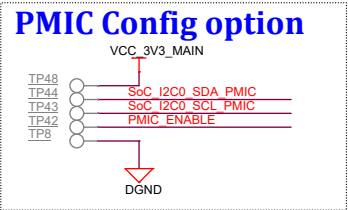


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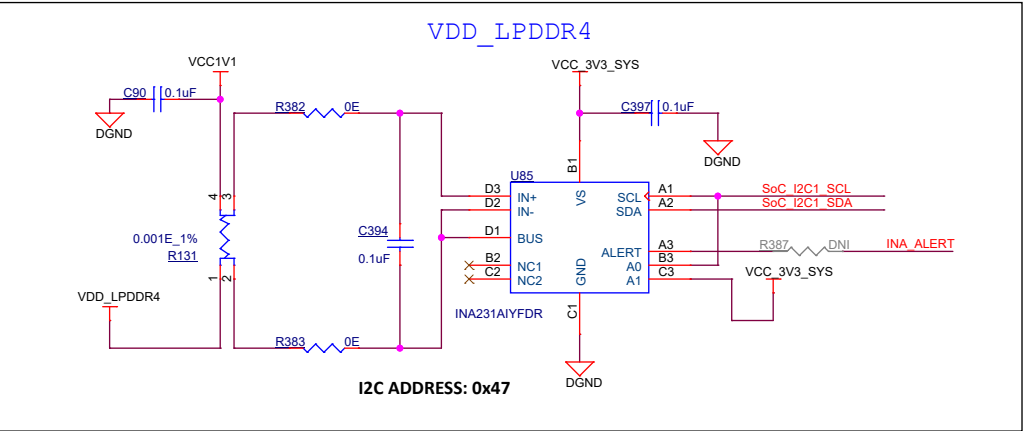
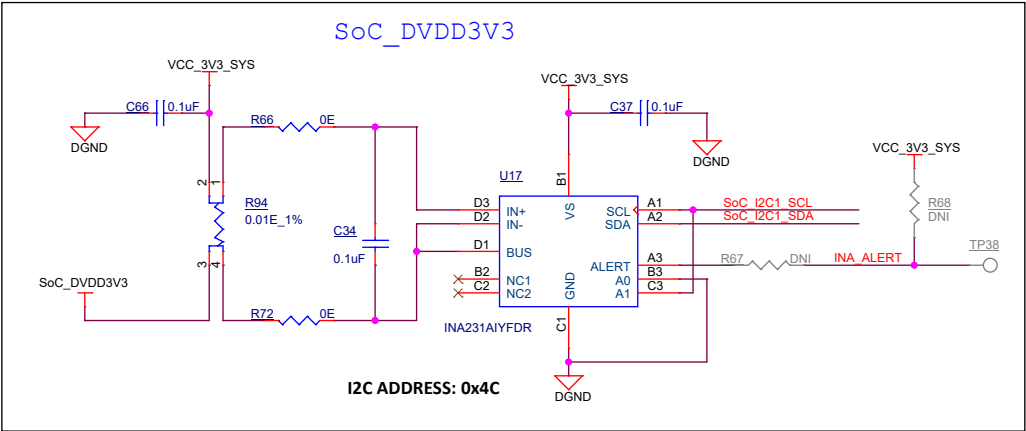
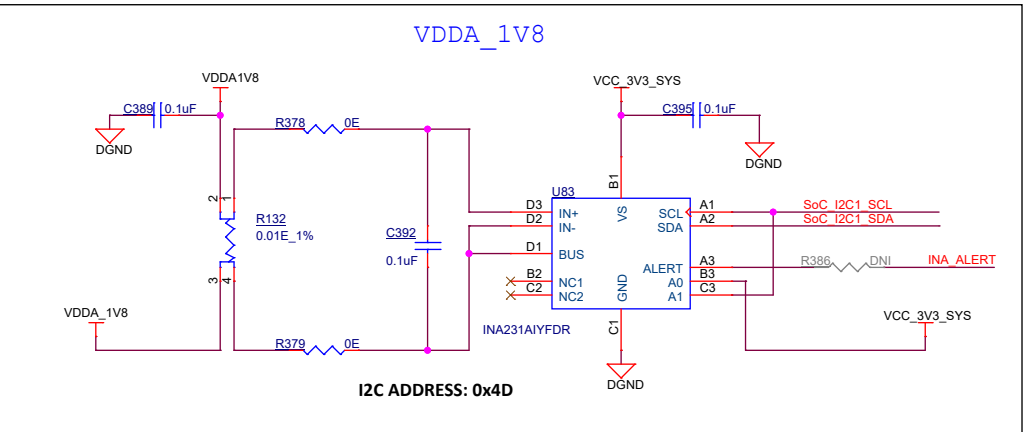
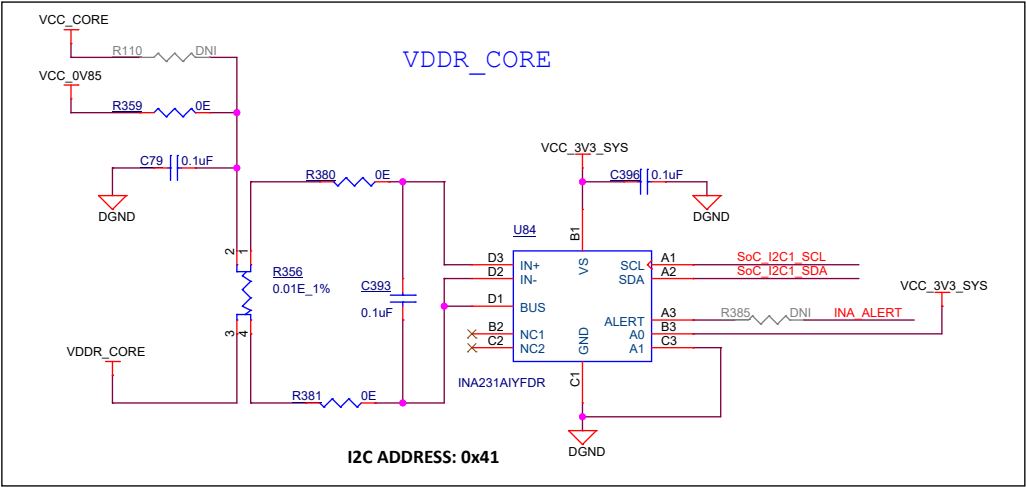
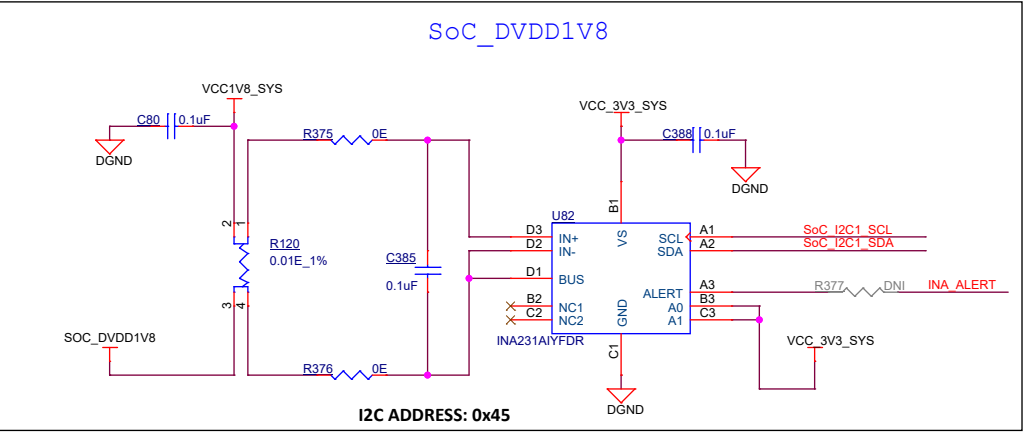
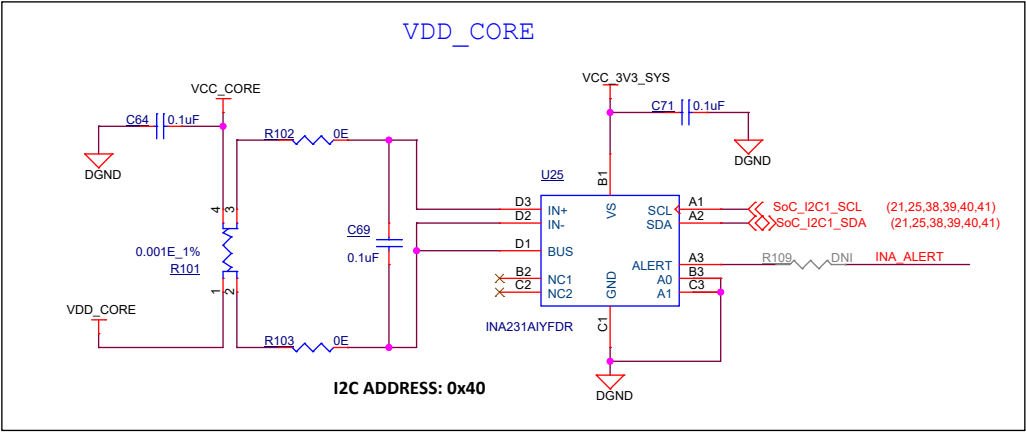


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SOC POWER SUPPLY PMIC

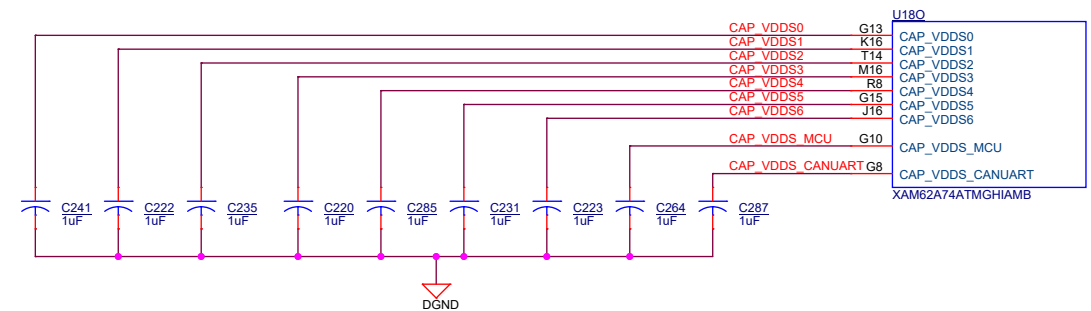
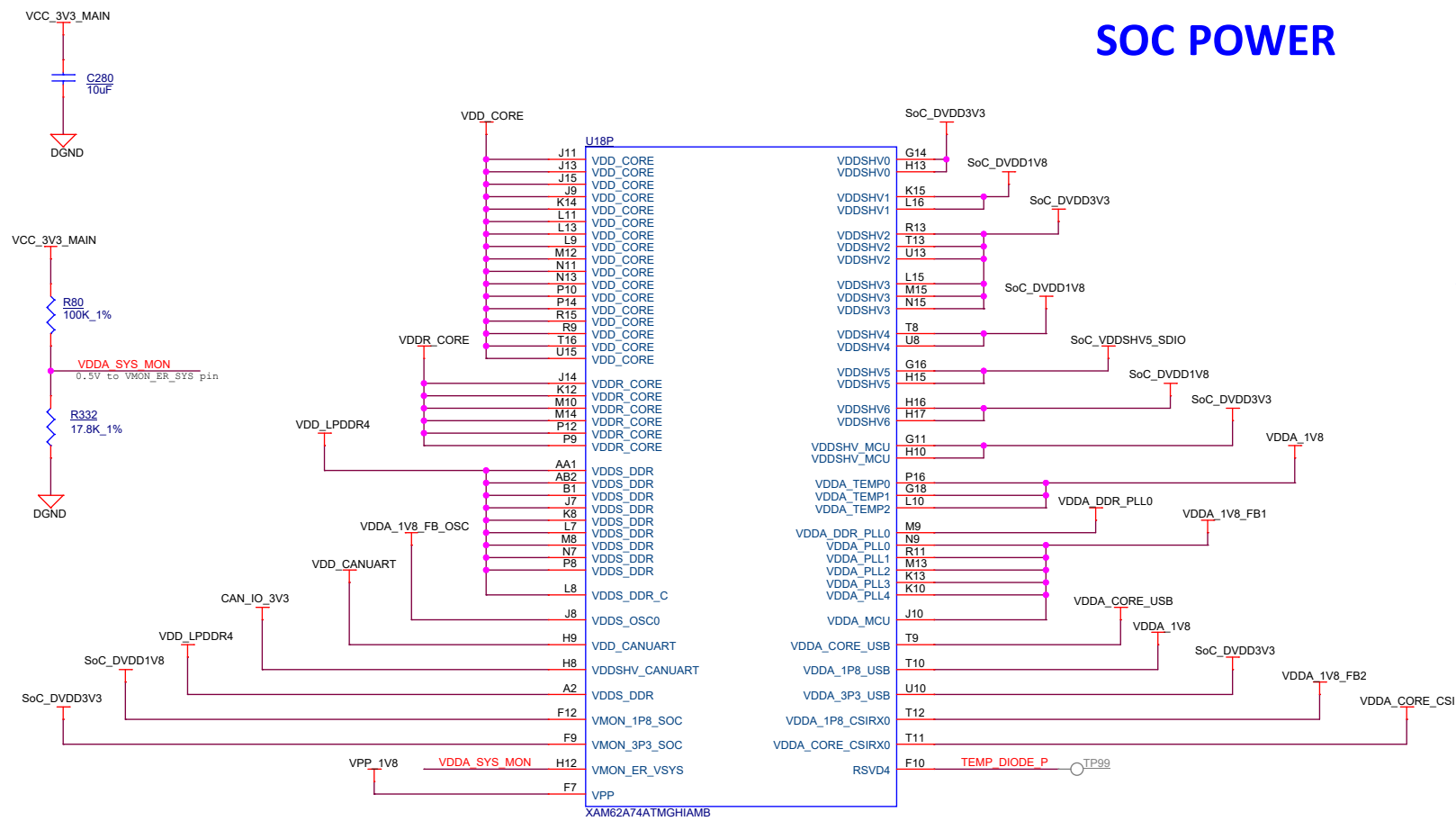


CURRENT MONITORING DEVICES

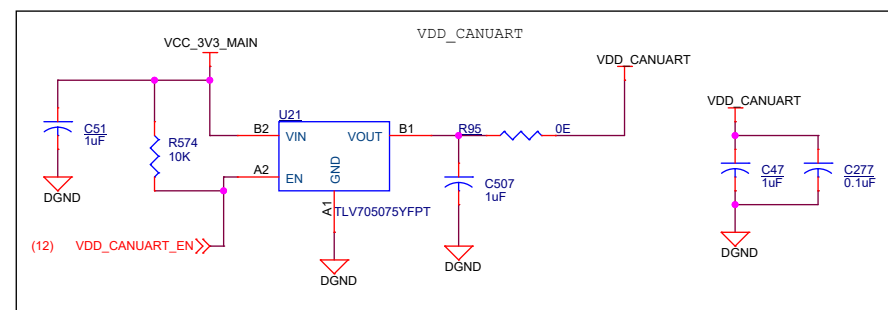
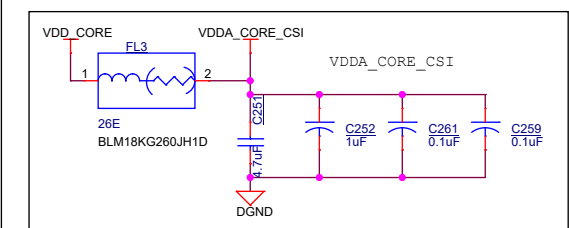
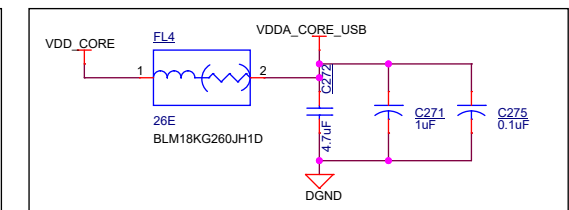
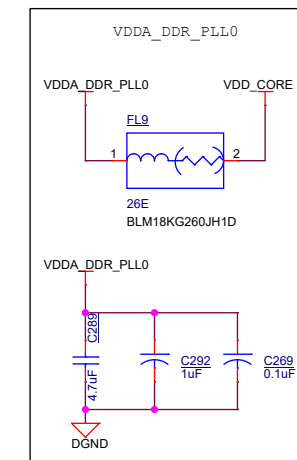
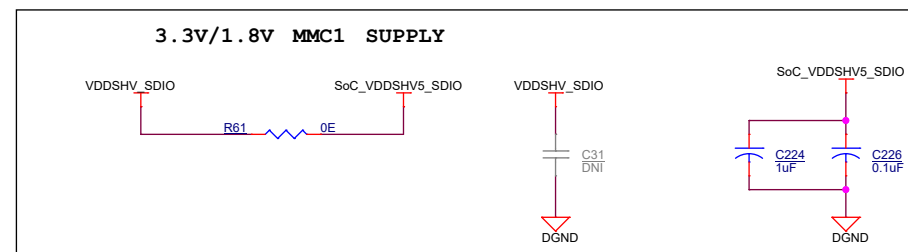
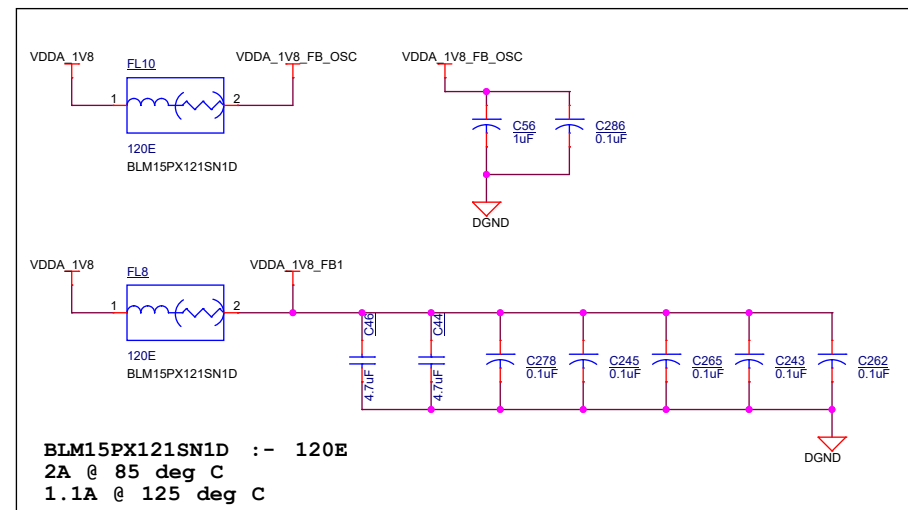
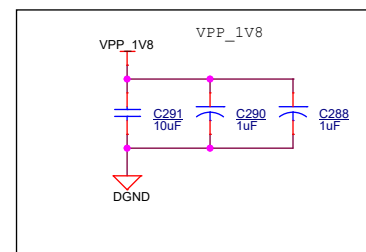
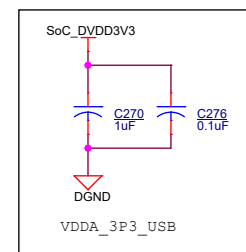
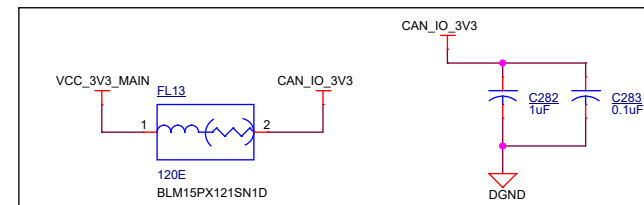
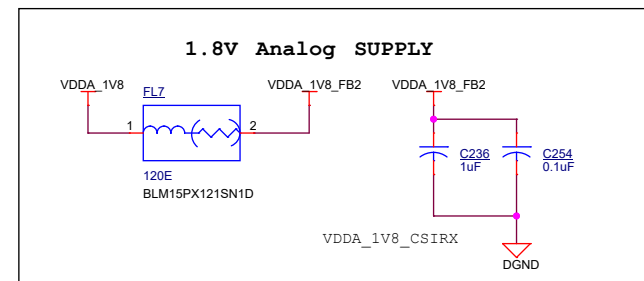


INA I2C SLAVE ADDRESS		
POWER SOURCE	SUPPLY NET	SLAVE ADDRESS (IN HEX)
VCC_CORE	VDD_CORE	40
VCC_0V85	VDDR_CORE	41
VCC_3V3_SYS	SoC_DVDD3V3	4C
VCC_1V8	SoC_DVDD1V8	45
VDDA1V8	VDDA_1V8	4D
VCC1V1	VDD_LPDDR4	47

SOC POWER



CORE SUPPLY



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Title	SOC POWER
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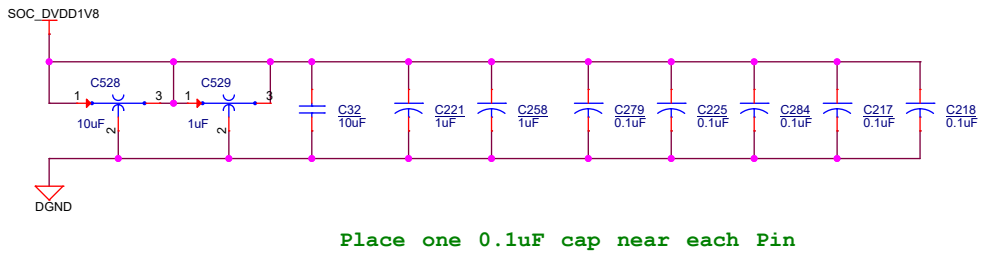
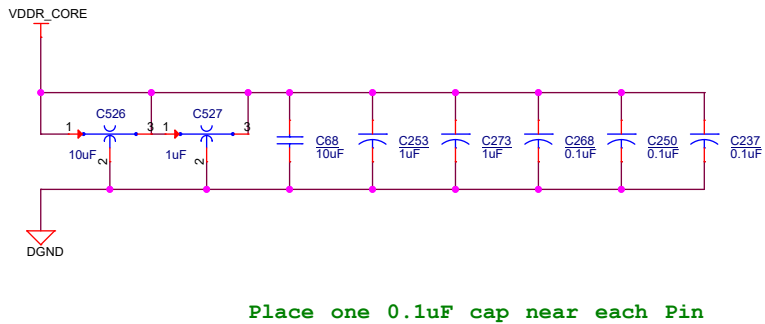
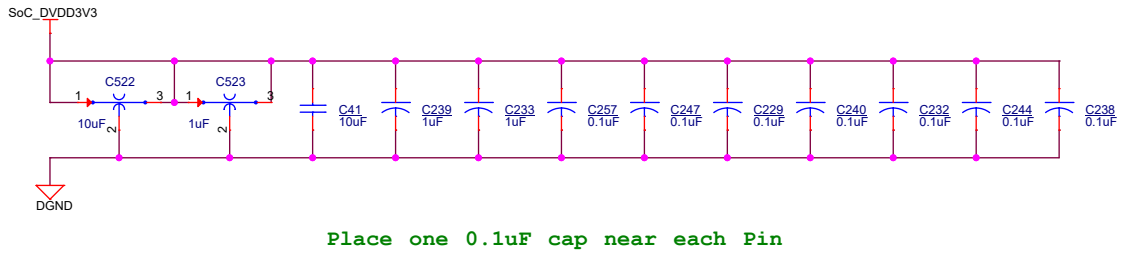
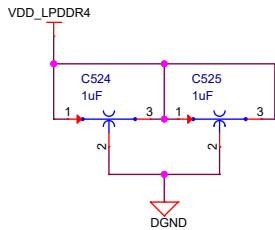
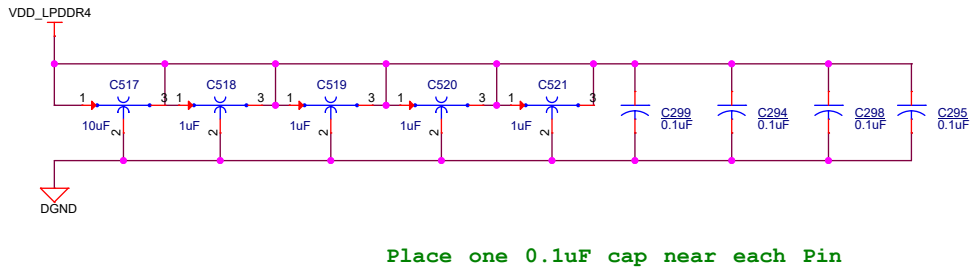
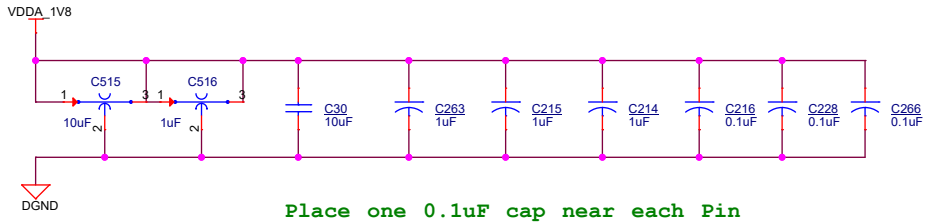
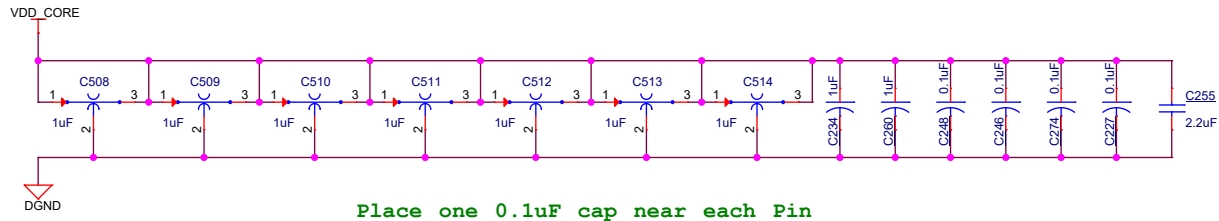
Size	PROC135E2
C	

Date: Monday, September 26, 2022

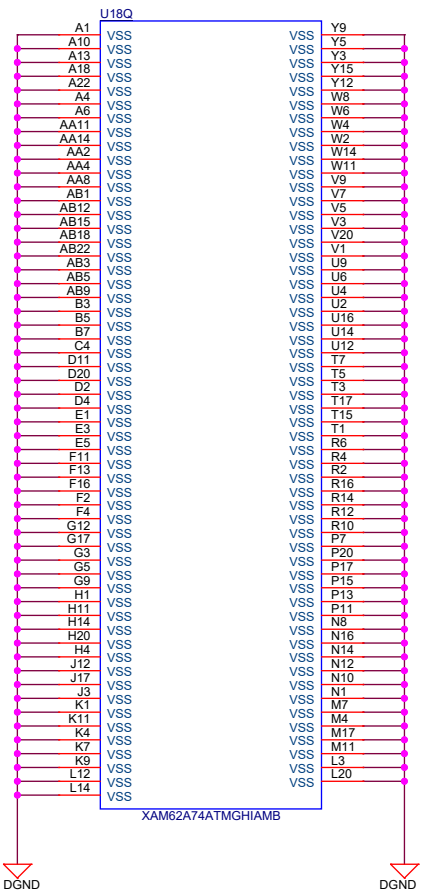
	I
	E

Sheet 14 of 44

SOC POWER DECAPS



SOC VSS



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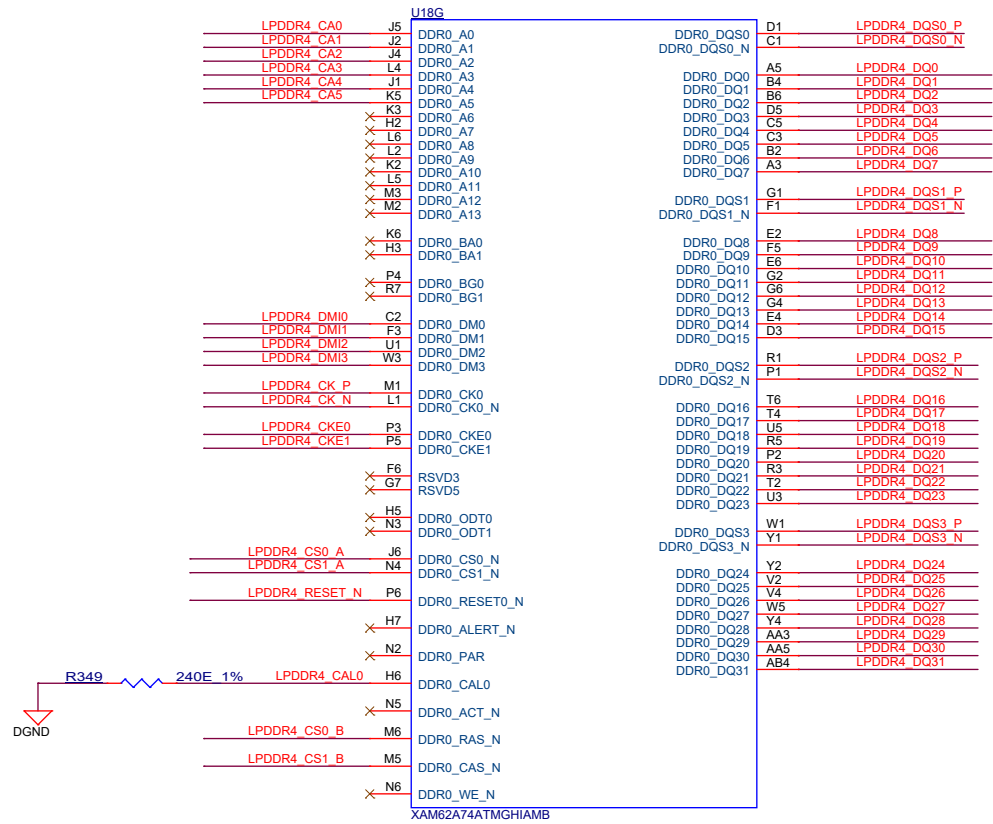


Title SOC POWER CAPS & SOC VSS

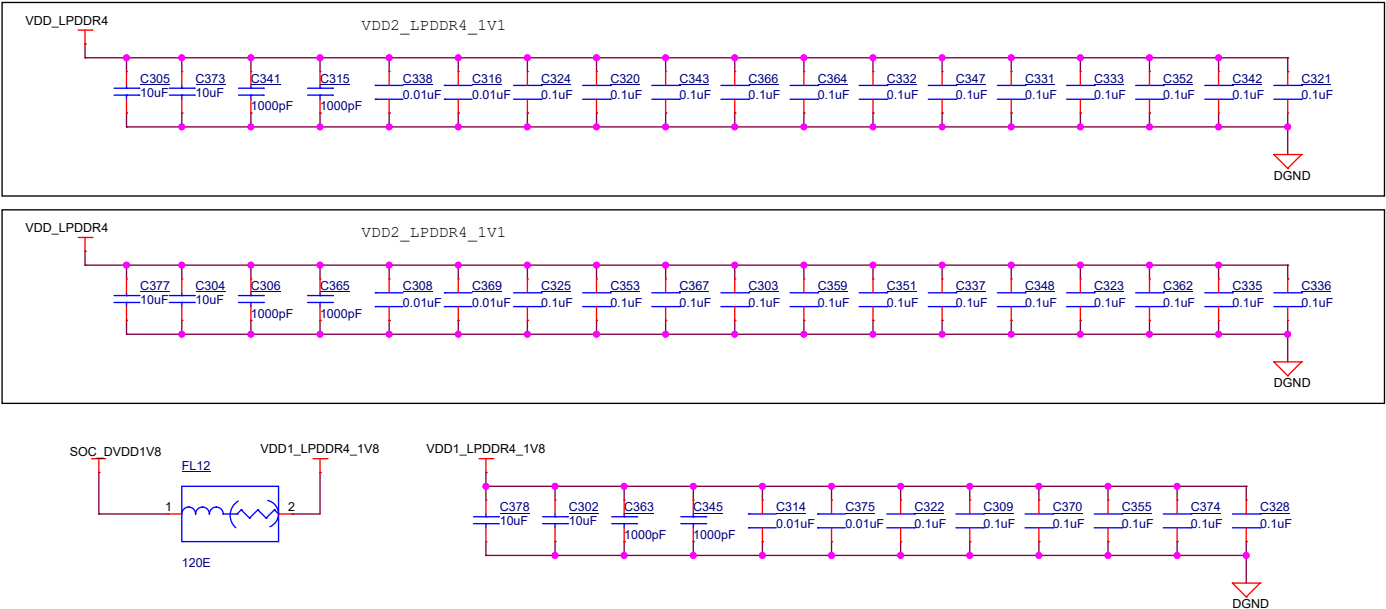
Size	Rev
C	PROC135E2
Date:	Tuesday, November 15, 2022

Sheet 15 of 44

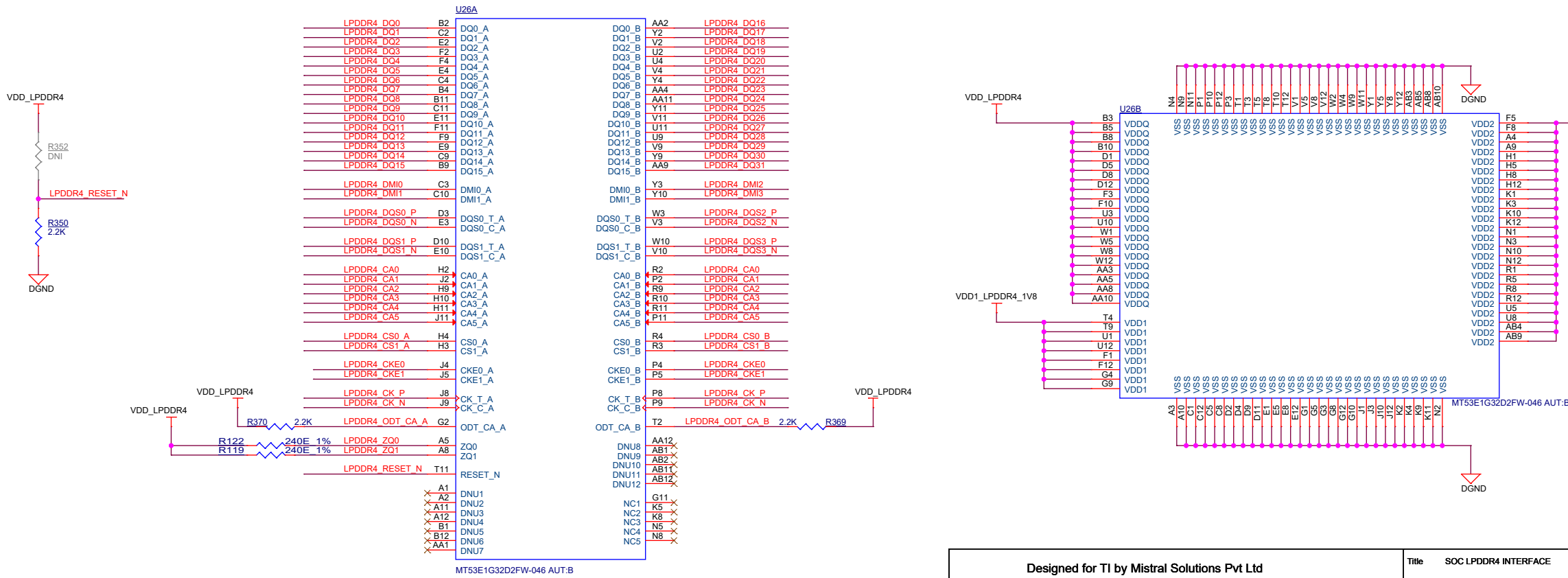
SOC LPDDR4 INTERFACE



LPDDR4 POWER DECAPS



LPDDR4 DEVICE



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Title SOC LPDDR4 INTERFACE

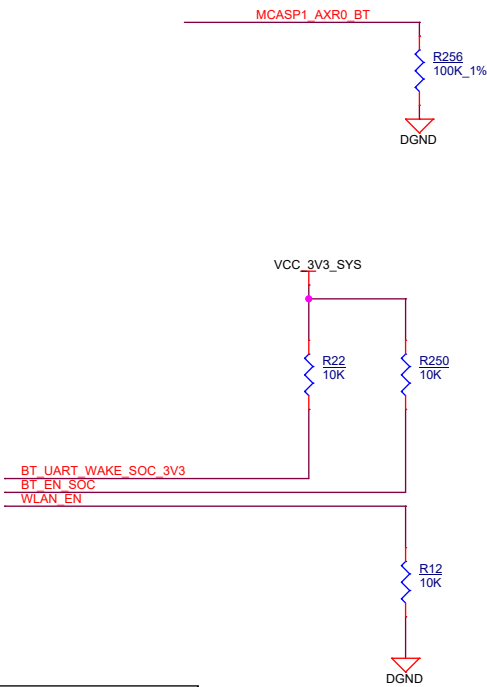
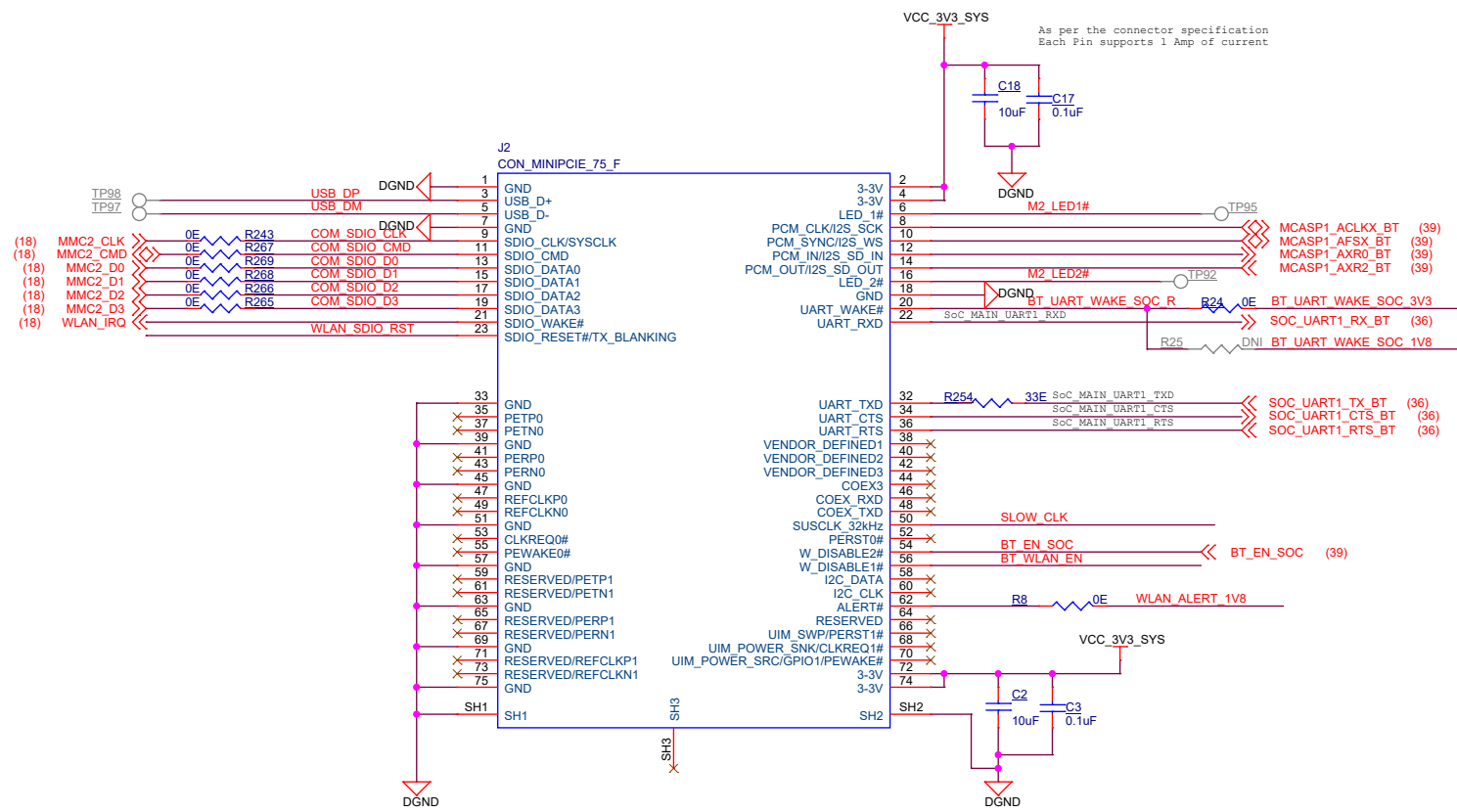
Size
C PROC135E2

Date: Tuesday, November 15, 2022

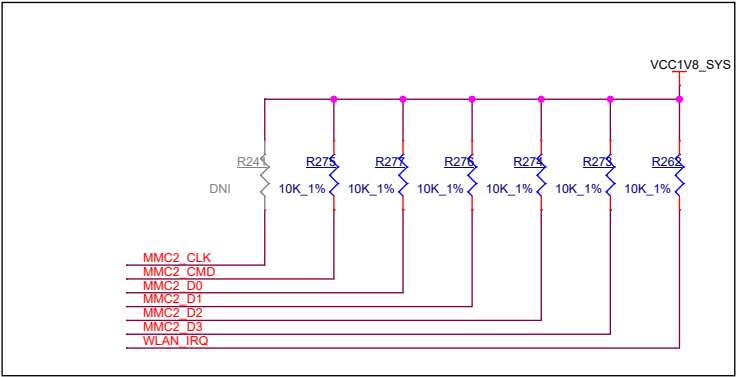
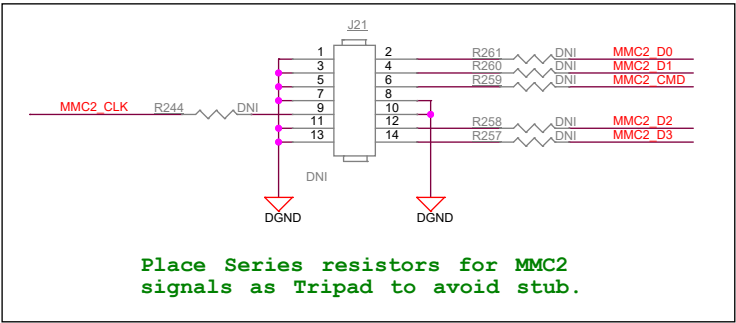
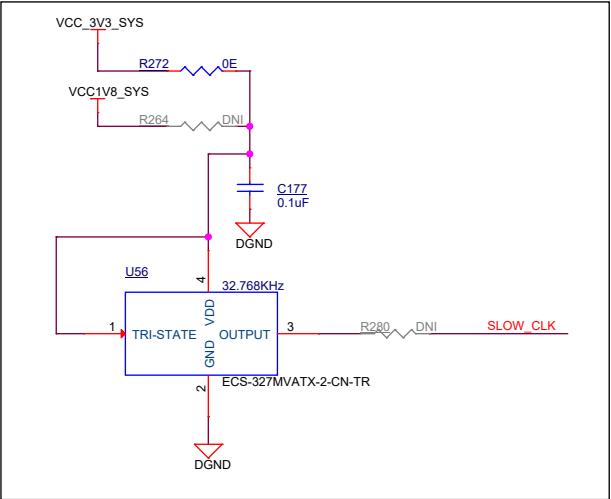
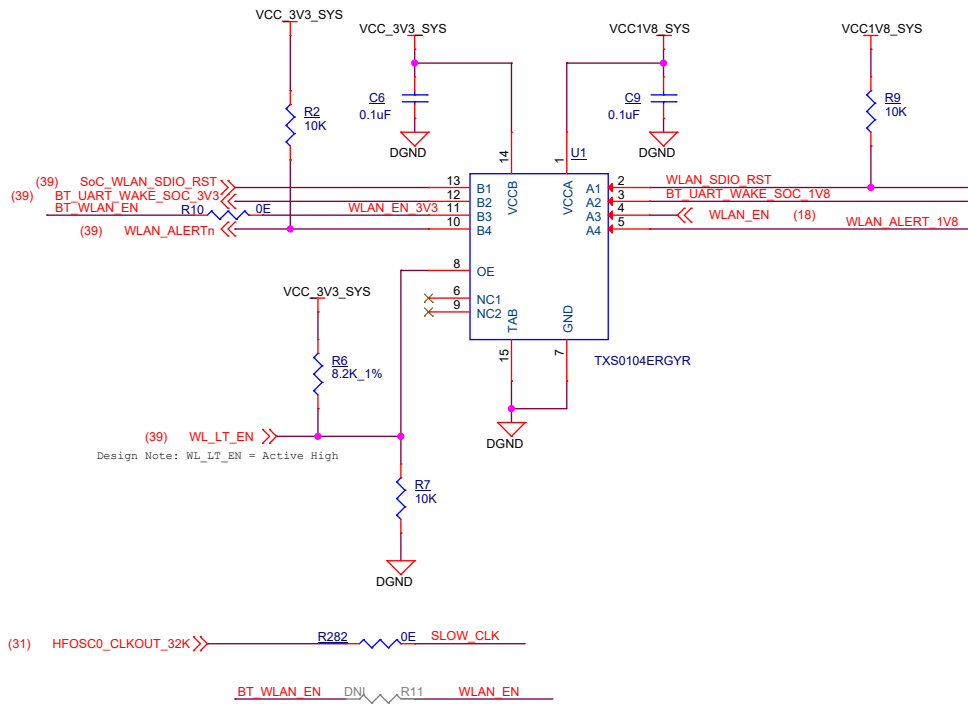
Sheet 16 of 44

Rev
E2

M.2 INTERFACE - SDIO



M.2 LEVEL TRANSLATOR

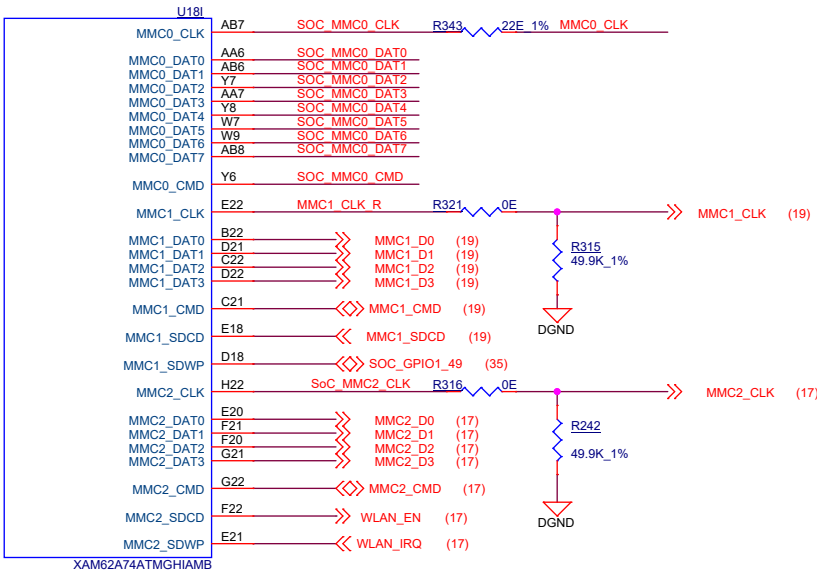


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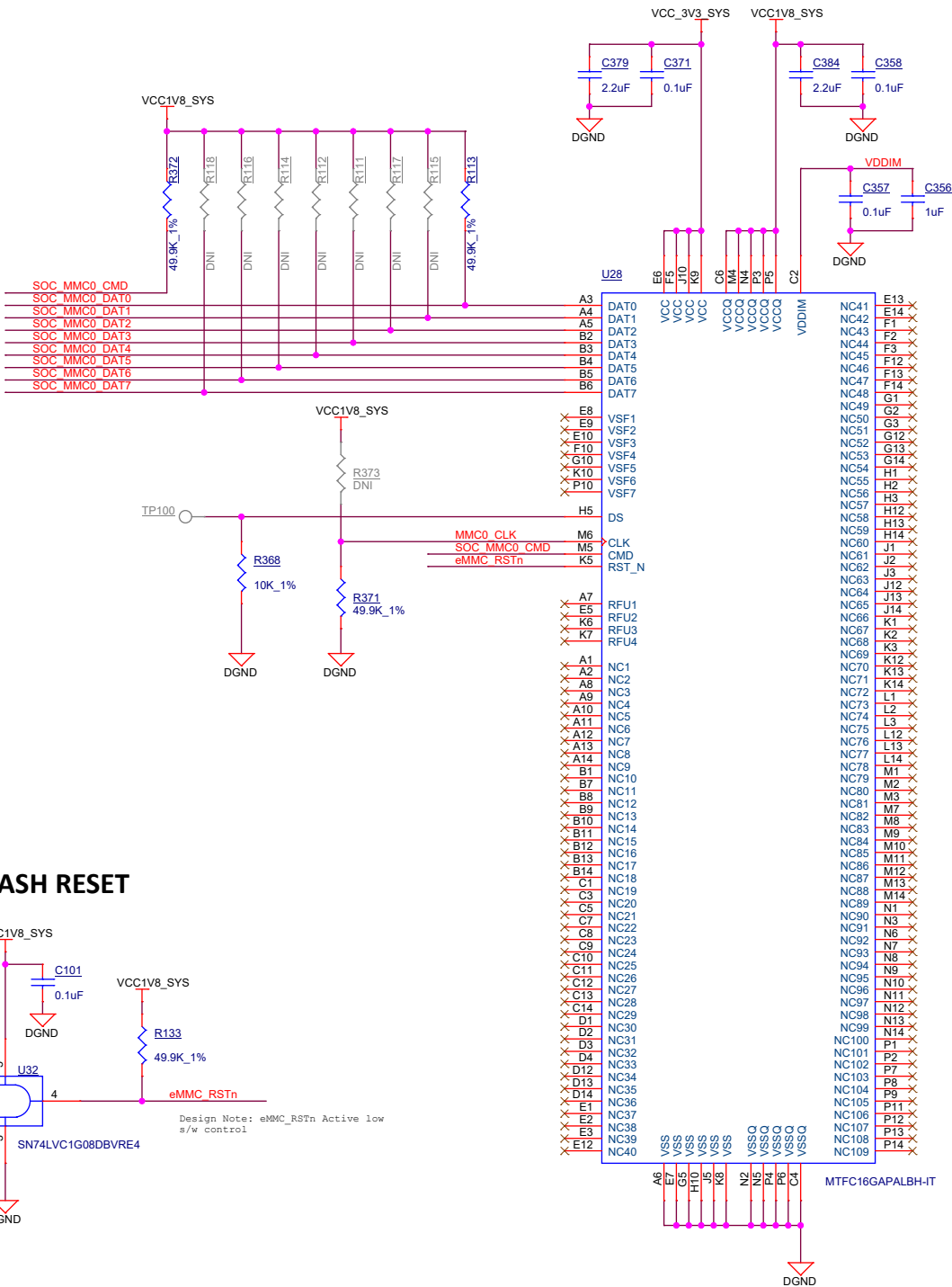


Title M.2 CONNECTOR I/F		
Size C	PROC135E2	Rev E2
Date: Monday, September 26, 2022	Sheet 17 of 44	

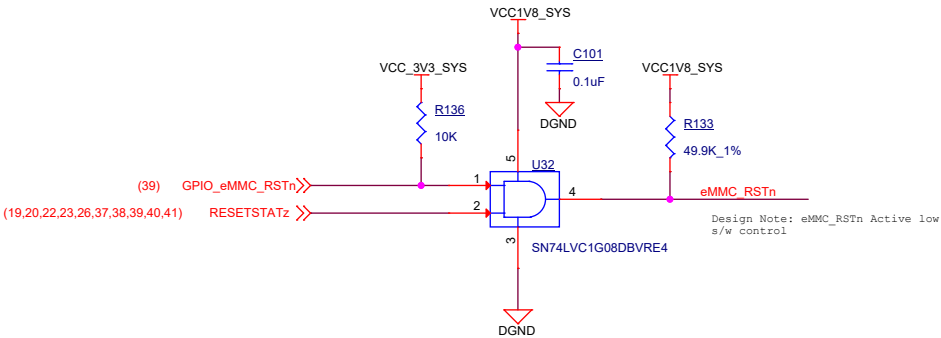
SOC - MMC Interface



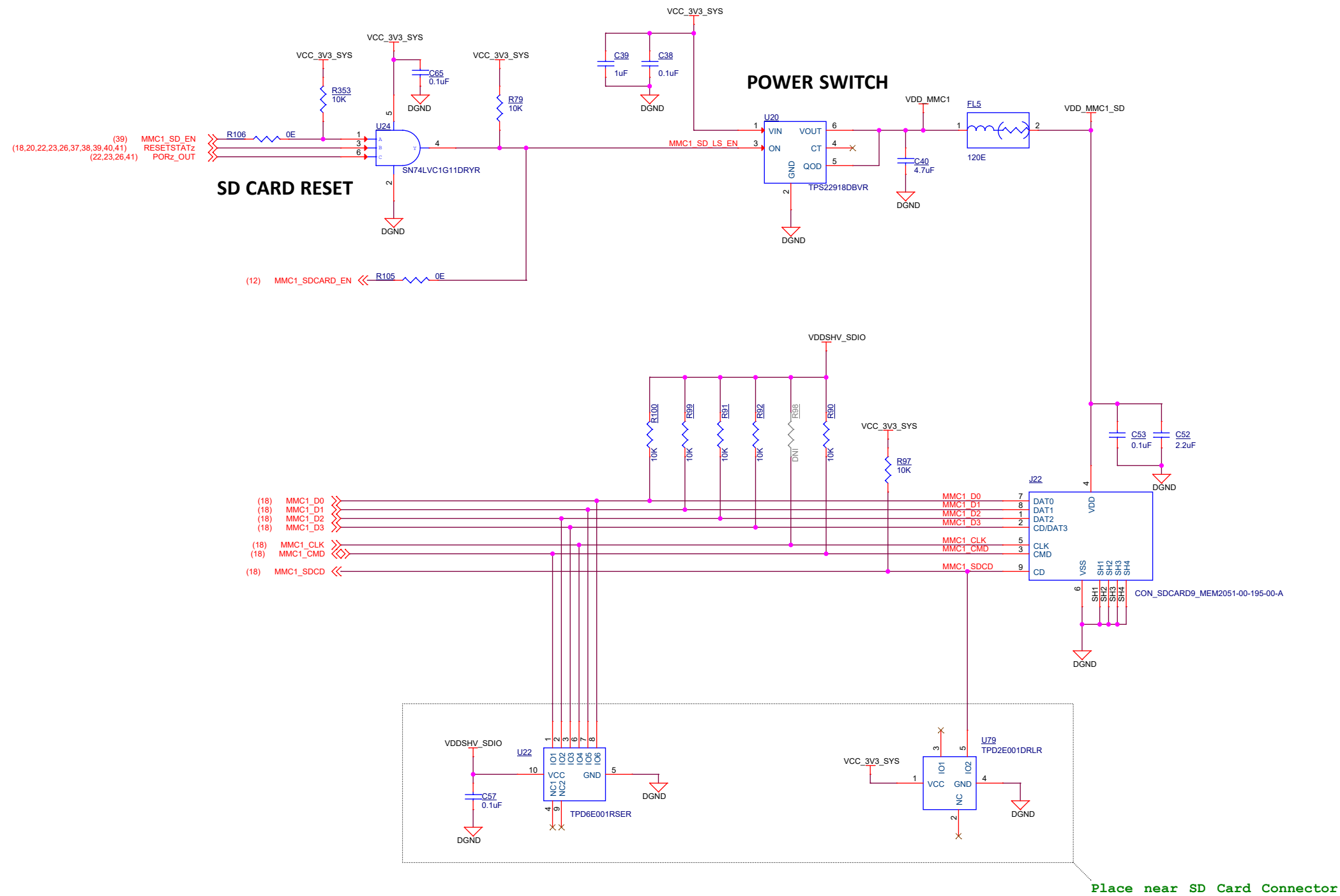
eMMC FLASH



eMMC FLASH RESET

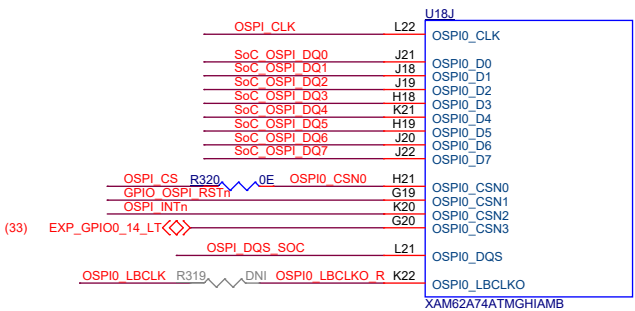
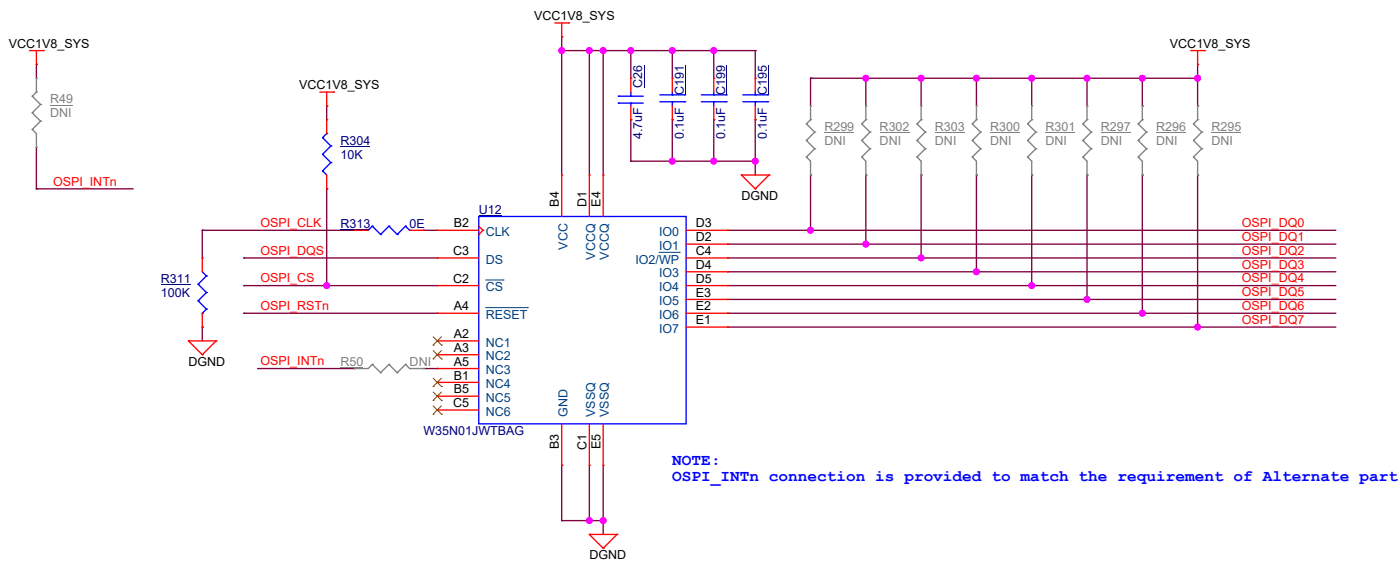


SD CARD INTERFACE

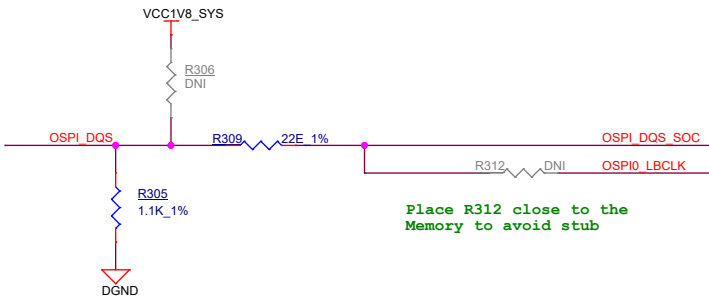
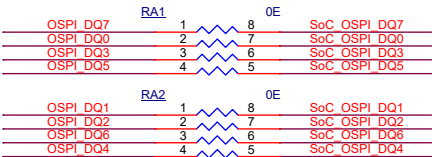
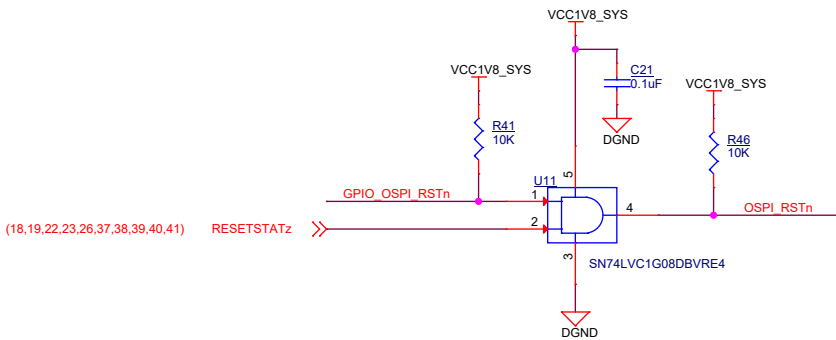


OSPI FLASH

SOC OSPI INTERFACE



OSPI FLASH RESET



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Title OSPI INTERFACE

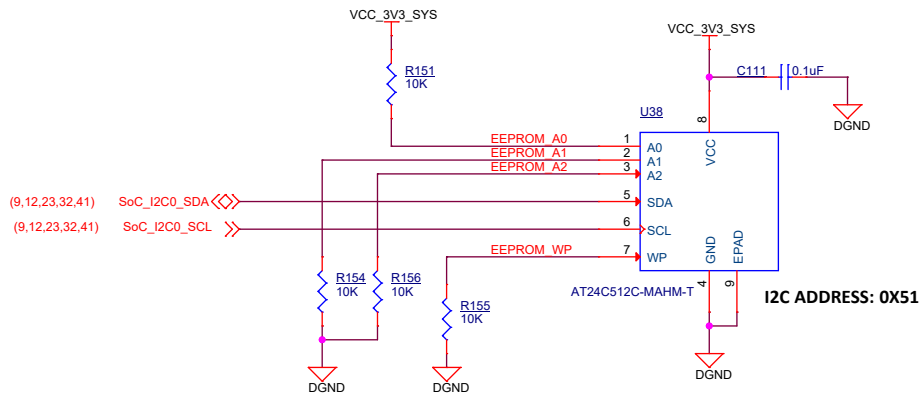
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Date: Monday, September 26, 2022

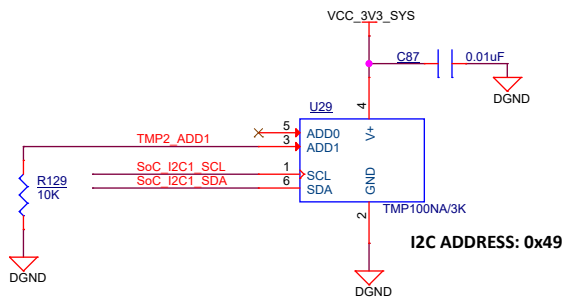
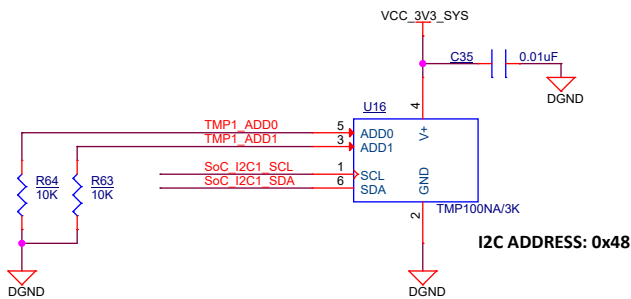
Sheet 20 of 44

Rev E2

BOARD ID EEPROM



TEMPERATURE SENSORS



CAD NOTE: PLACE TEMP SENSOR U16 CLOSE TO SoC

CAD NOTE: PLACE TEMP SENSOR U29 CLOSE TO DDR4

(13,25,38,39,40,41) SoC_I2C1_SCL >> TP49
(13,25,38,39,40,41) SoC_I2C1_SDA <<< TP50
Silk: SOC_I2C1

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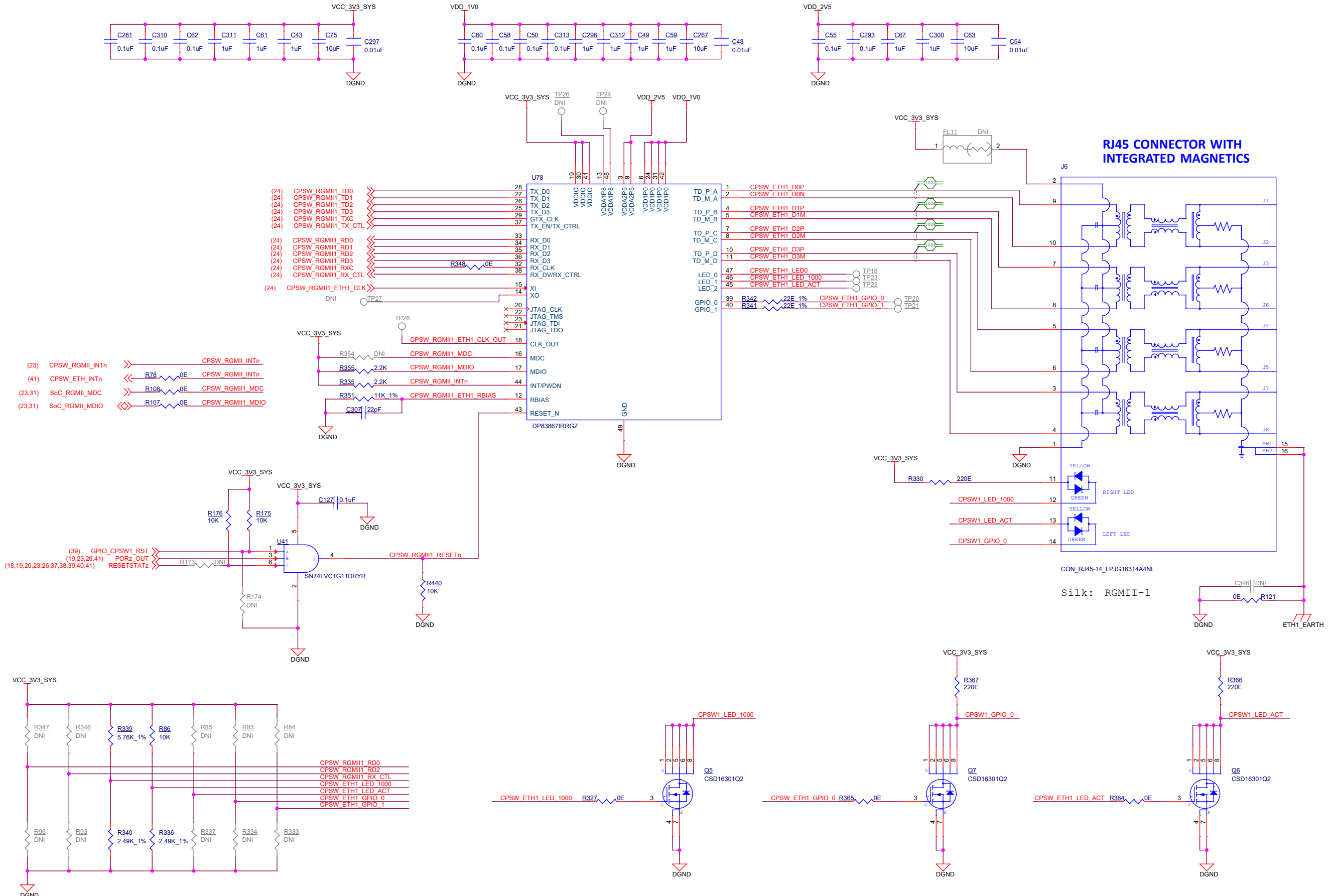
Title BOARD ID EEPROM & TEMPERATURE SENSORS

Size C
PROC135E2

Rev E2

Date: Monday, September 26, 2022 Sheet 21 of 44

CPSW RGMII 1 - PHY



```
PHY ADDRESS = 00000
Auto-negotiation Enabled
10/100/1000 advertised, Auto-MDI-X
Tx Clock Skew = 0ns
Rx Clock Skew = 2ns
```

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Title	CPSW RGMII_1 ETHERNET PHY
-------	---------------------------

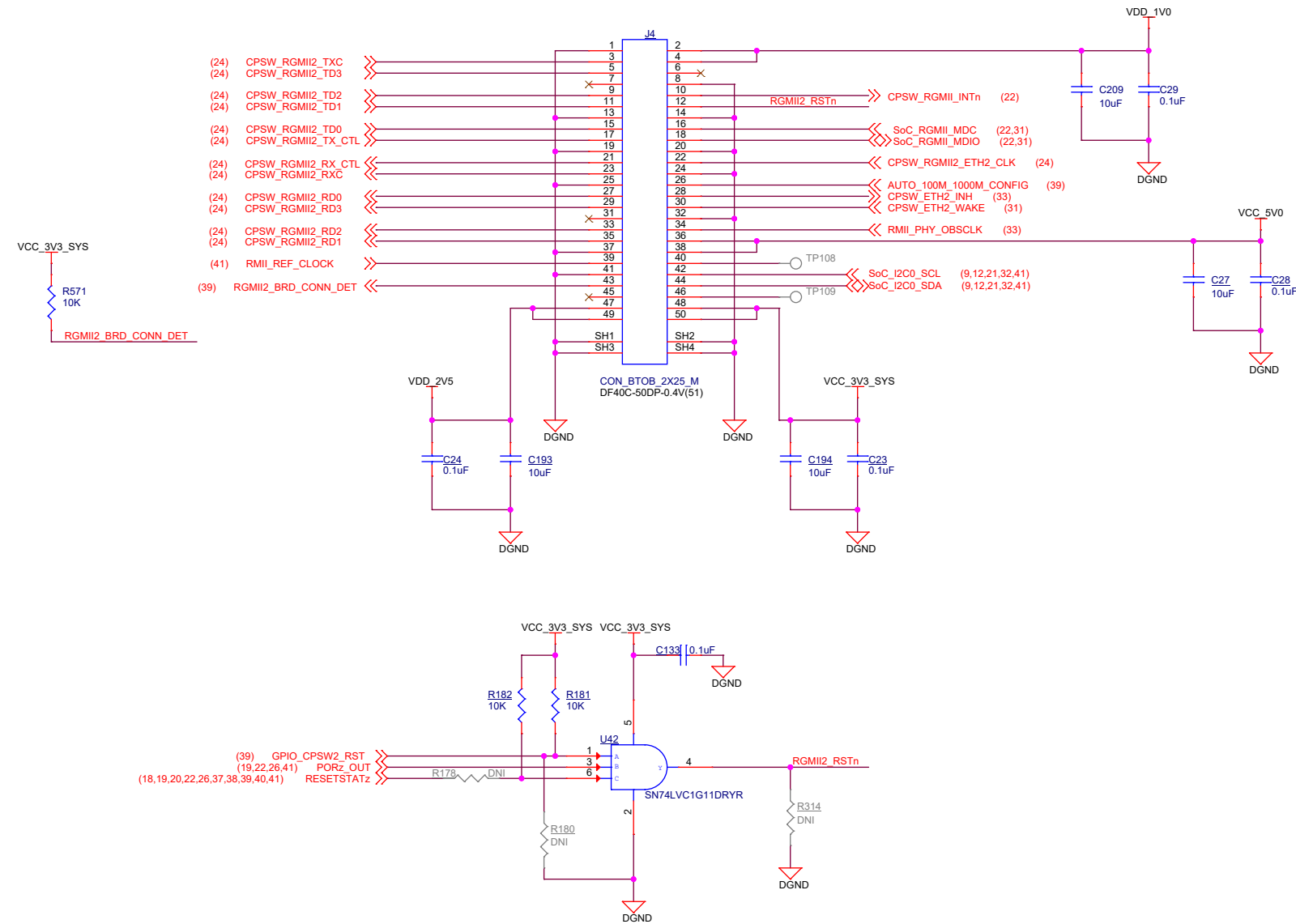
Size	PROC135E2
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Rev

Date: Monday, September 26, 2022

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CPSW RGMII 2 - PHY



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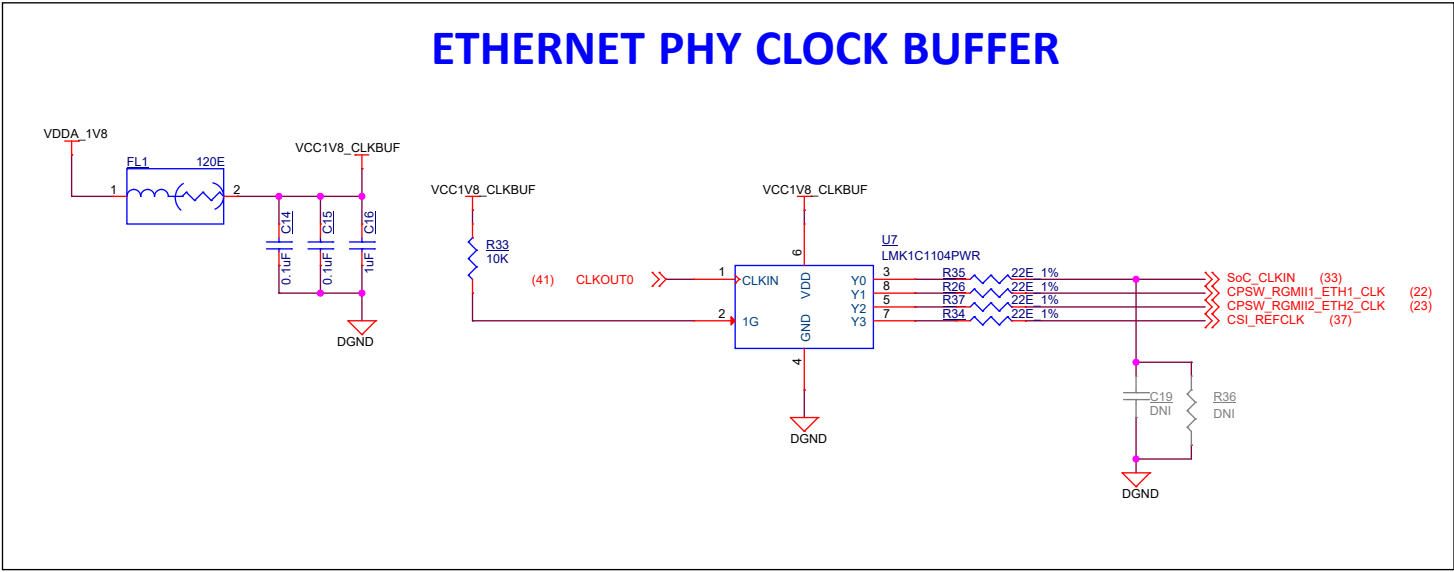
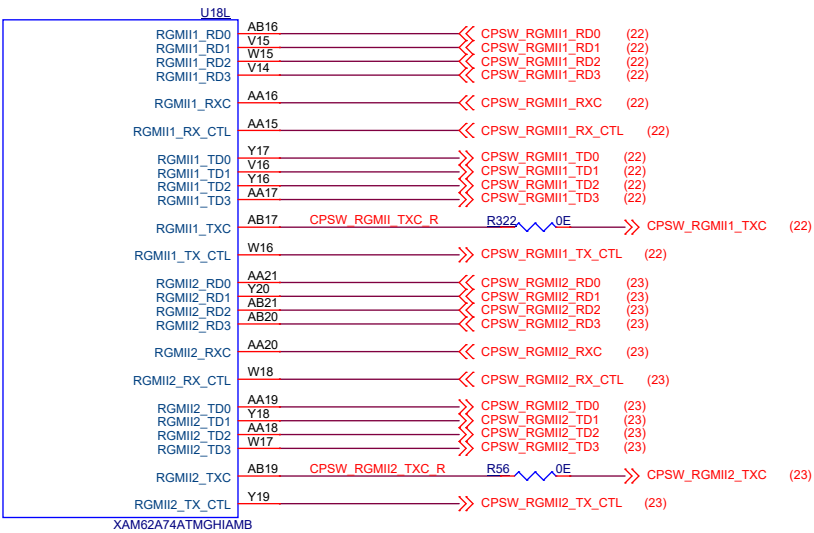
Title CPSW RMII_2 ETHERNET PHY

Size C
PROC135E2

Rev E2

Date: Monday, September 26, 2022

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Title ETHERNET PHY CLOCK BUFFER & LED DRIVER

Size
C PROC135E2

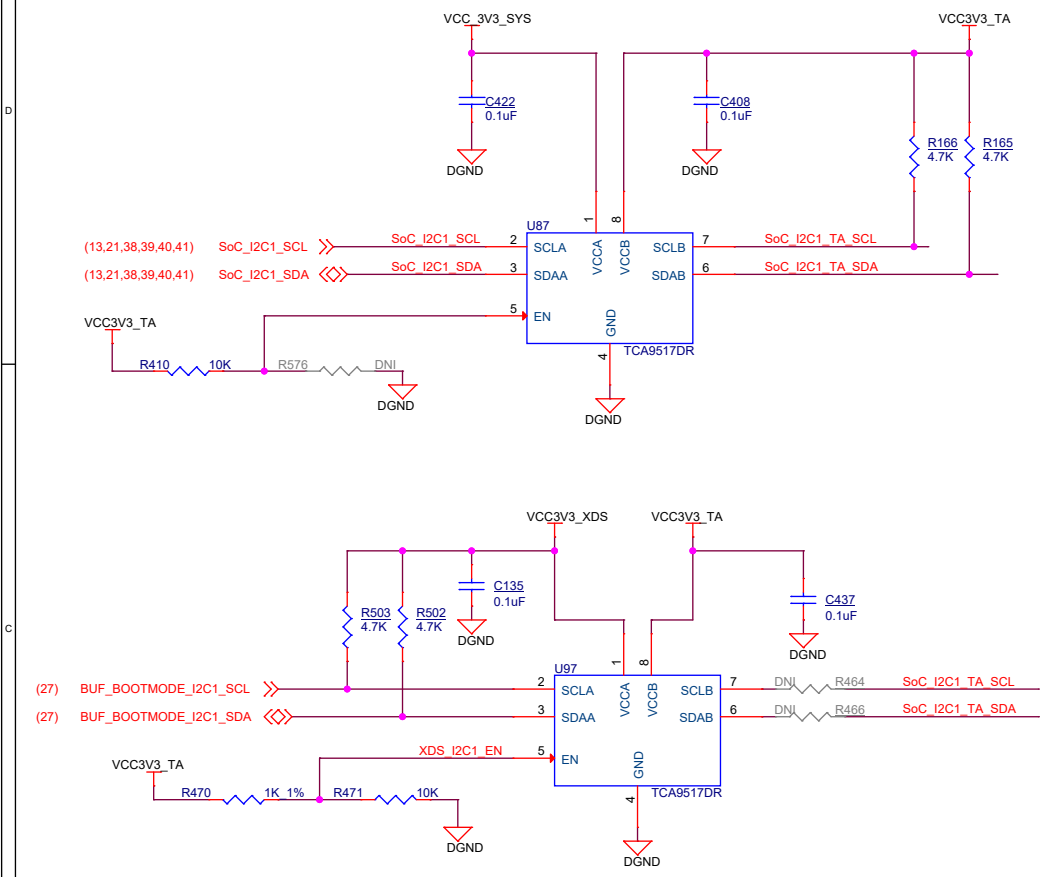
Rev

E2

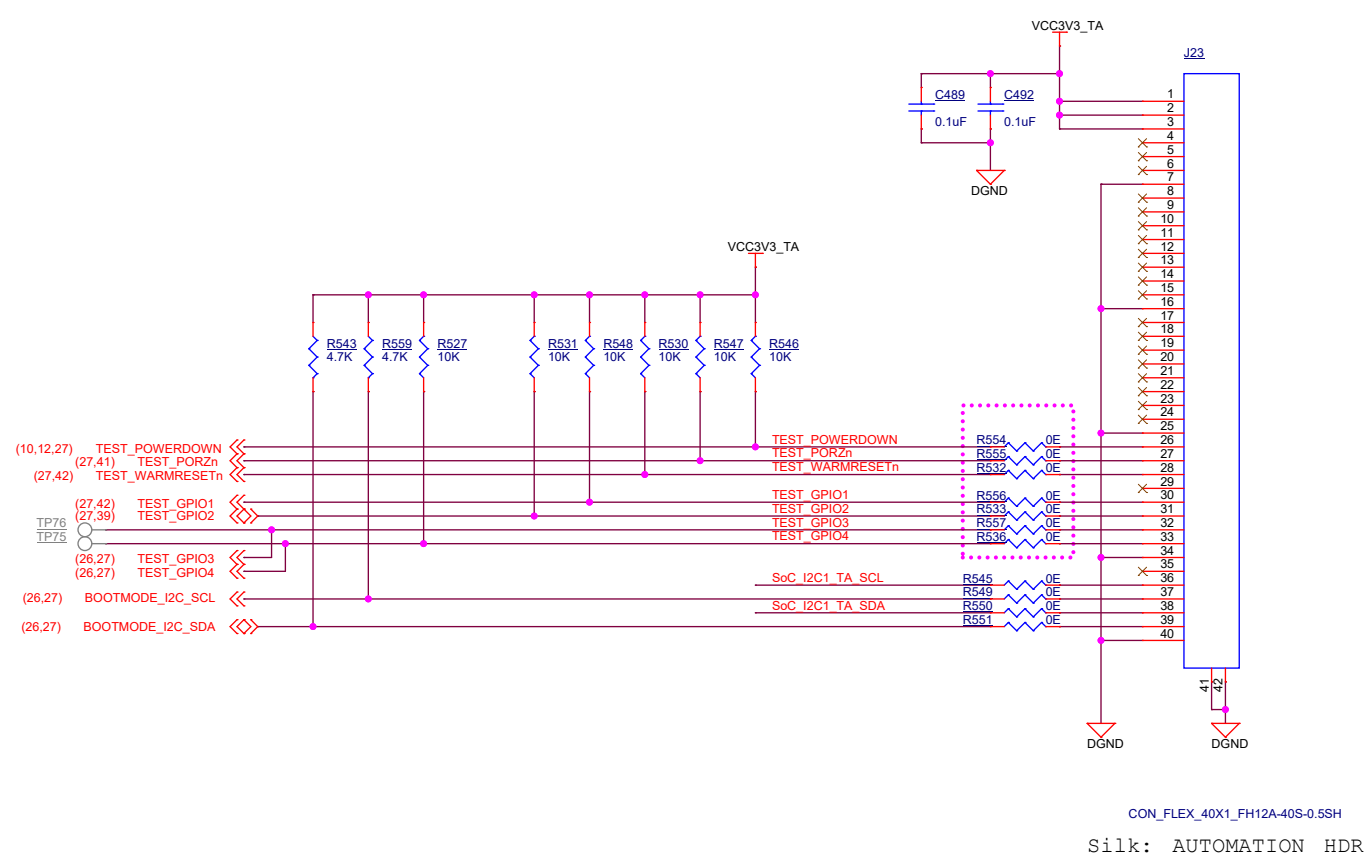
Date: Monday, September 26, 2022

Sheet 24 of 44

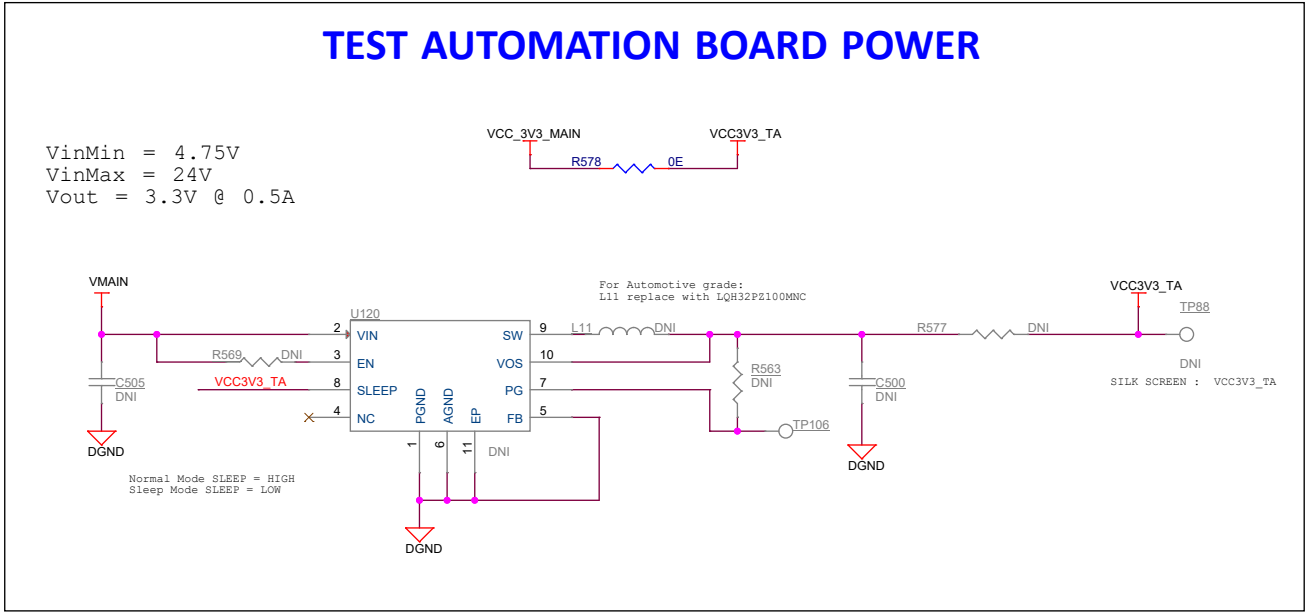
I2C BUS BUFFER



40-PIN TEST AUTOMATION HEADER



TEST AUTOMATION BOARD POWER



TEST AUTOMATION GPIO MAPPING

SIGNAL NAME	DESCRIPTION	Direction WRT CTRL	Internal/ External PU/PD states
TEST_POWERDOWN	Used to Power down the EVM	OUTPUT	External Pullup
TEST_PORZn	Used to Reset the SoC PORz	OUTPUT	External Pullup
TEST_WARMRESETn	Used to Reset the SoC Warmreset	OUTPUT	External Pullup
TEST_GPIO1	Used to Generate the interrupt on SOC_GPIO1_23 Pin	OUTPUT	External Pullup
TEST_GPIO2	Connected to IO Expander to Communicate with SOC	OUTPUT	External Pullup
TEST_GPIO3	Used to Enable the BOOTMODE Buffer	OUTPUT	External Pullup
TEST_GPIO4	Used to Reset the Bootmode I2C IO Expander	OUTPUT	External Pullup

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Title TEST AUTOMATION

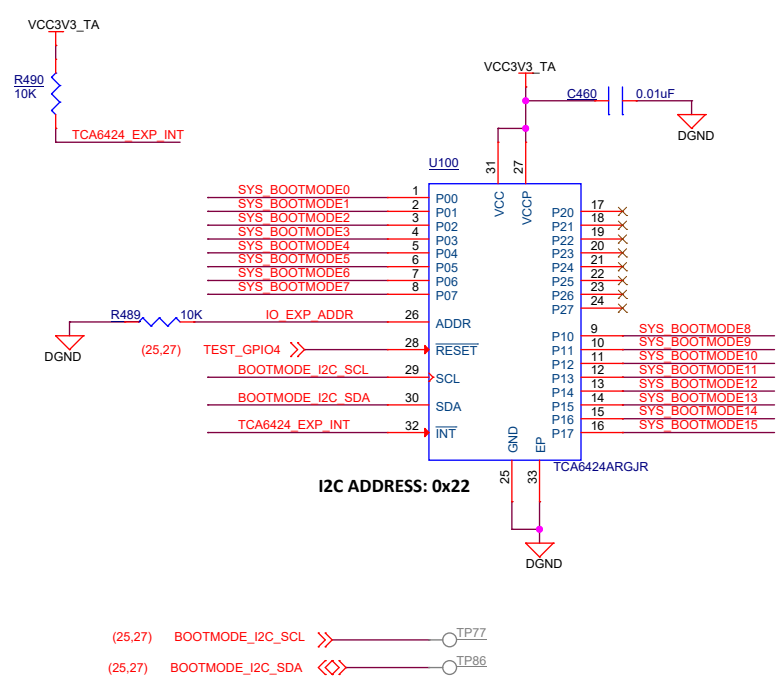
Size PROC135E2
C

Rev E2

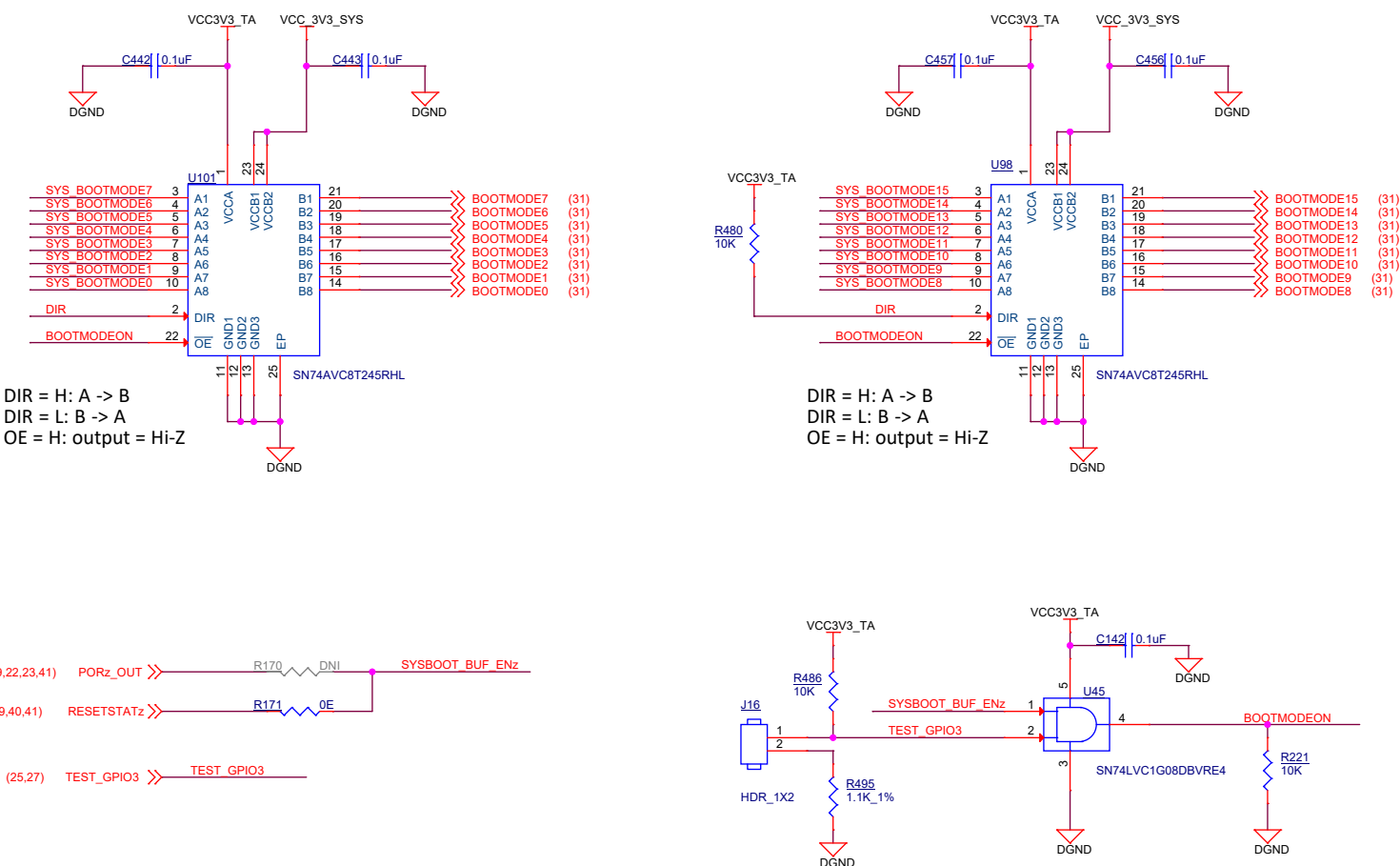
Date: Monday, September 26, 2022

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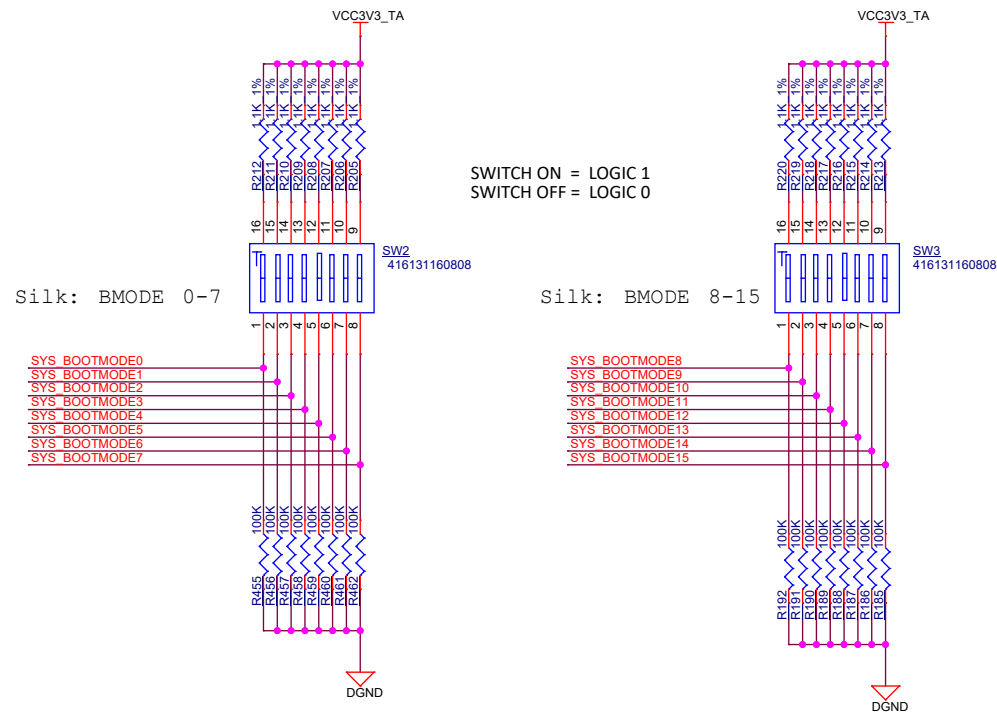
BOOTMODE IO EXPANDER



BOOT MODE BUFFERS

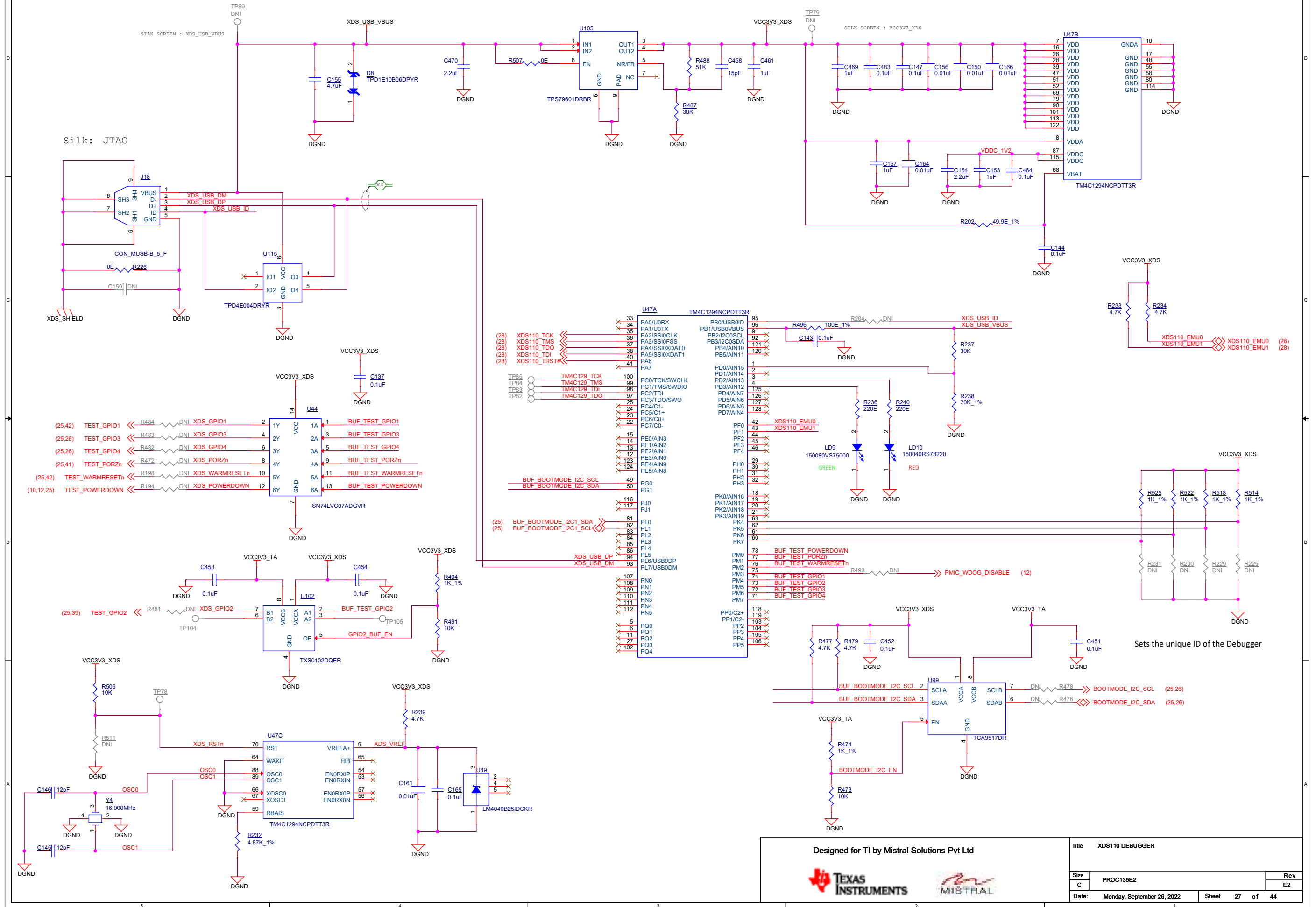


BOOT MODE SWITCHES

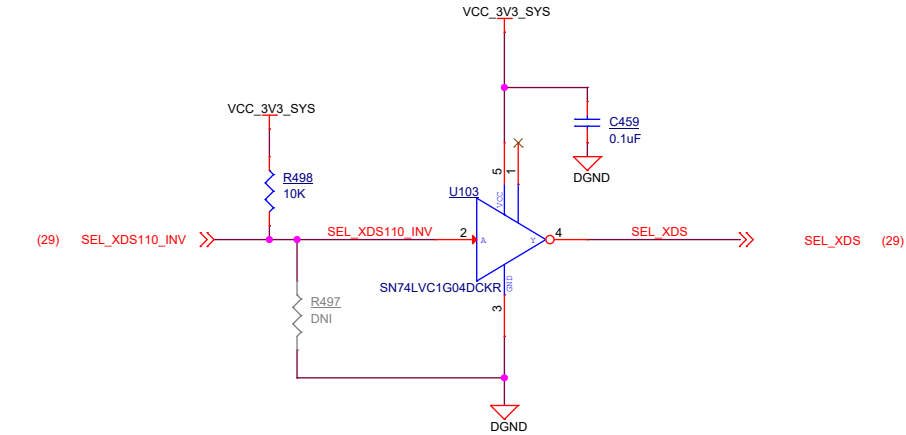
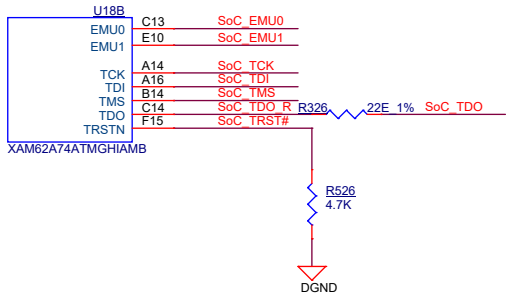


BOOT MODES SUPPORTED	
1.	OSPI
2.	MMC1 - SD CARD
3.	UART
4.	eMMC
5.	ETHERNET
6.	USB0 DFW
7.	USB0 MS

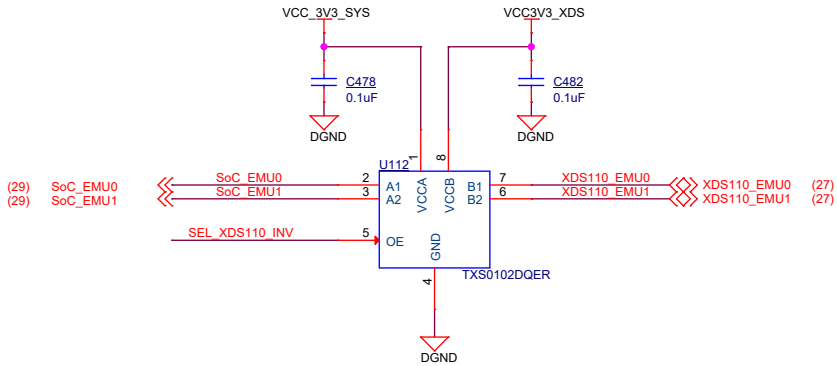
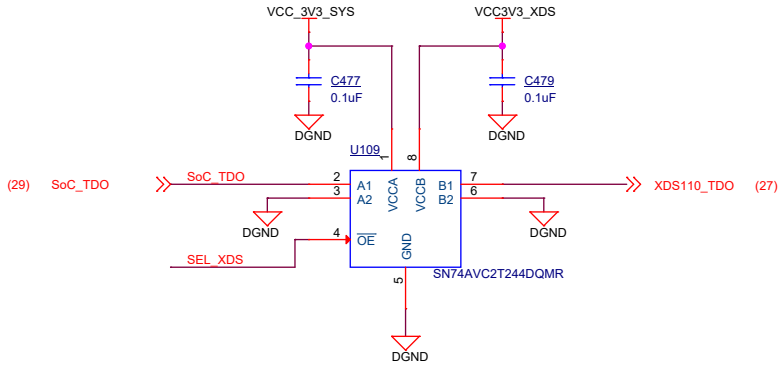
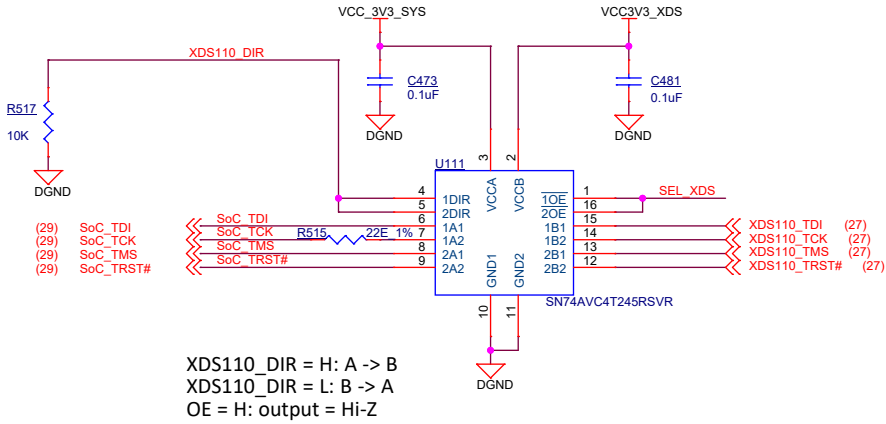
XDS110 DEBUGGER



JTAG SOC SECTION



BUFFER XDS110



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Title JTAG BUFFER

Size PROC135E2

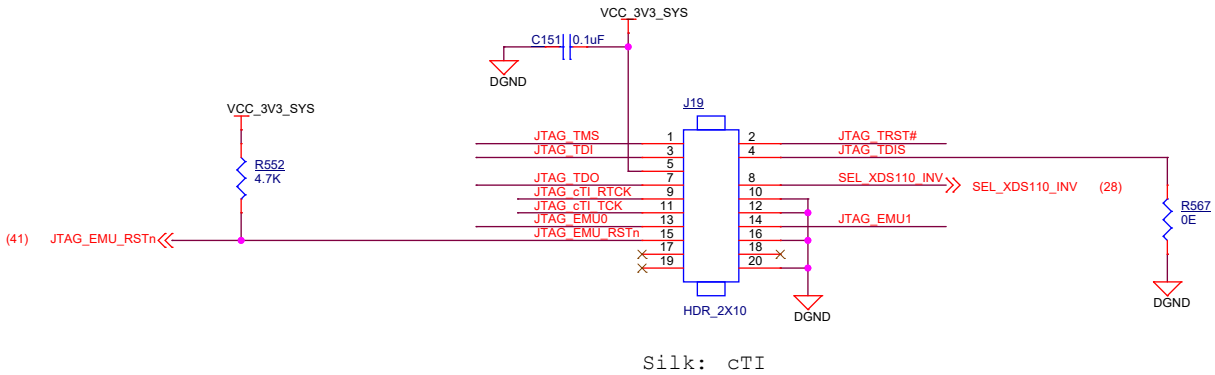
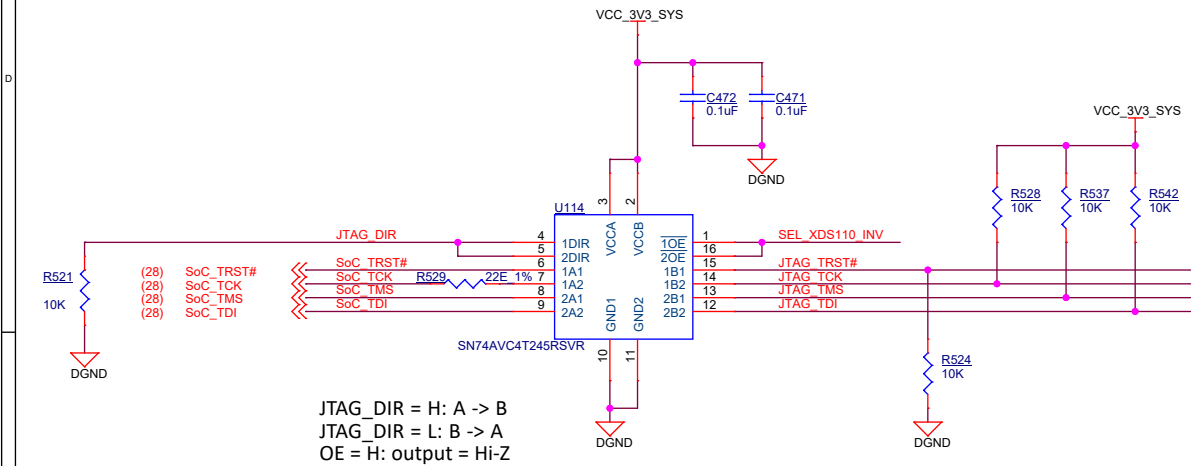
Date: Monday, September 26, 2022

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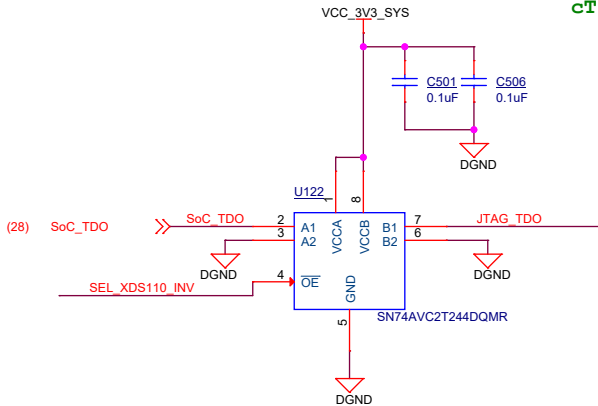
Rev E2

cTI20 JTAG BUFFERS

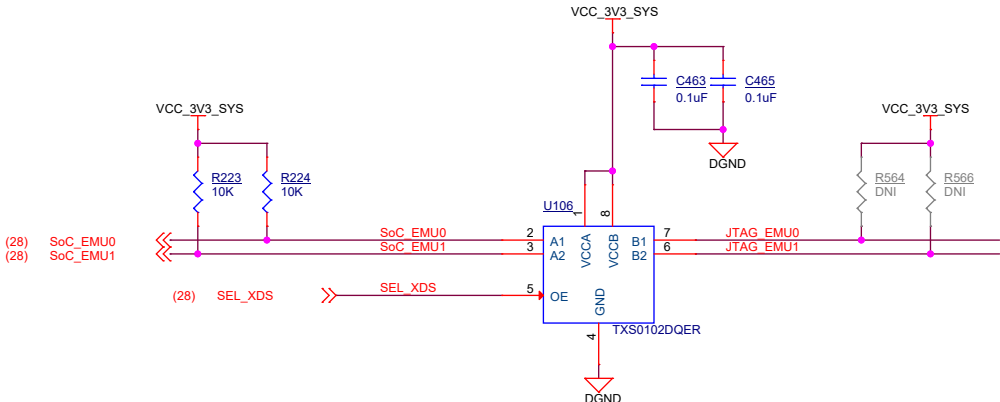
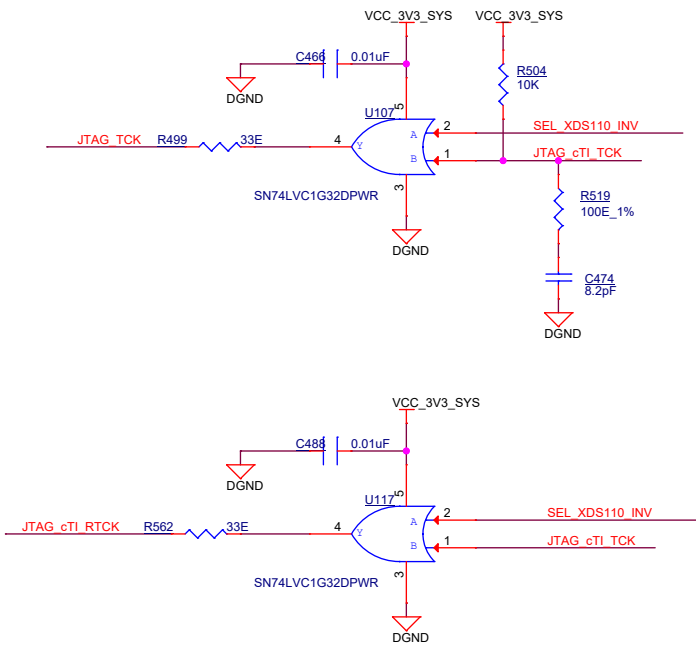
JTAG 20 PIN cTI CONNECTOR



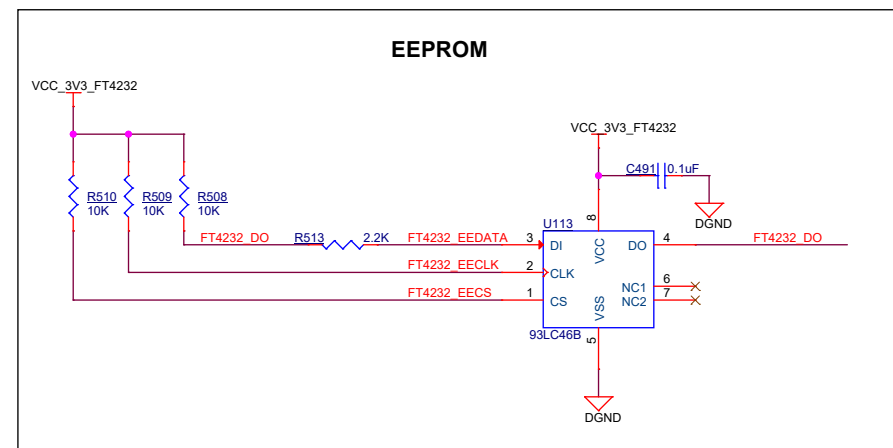
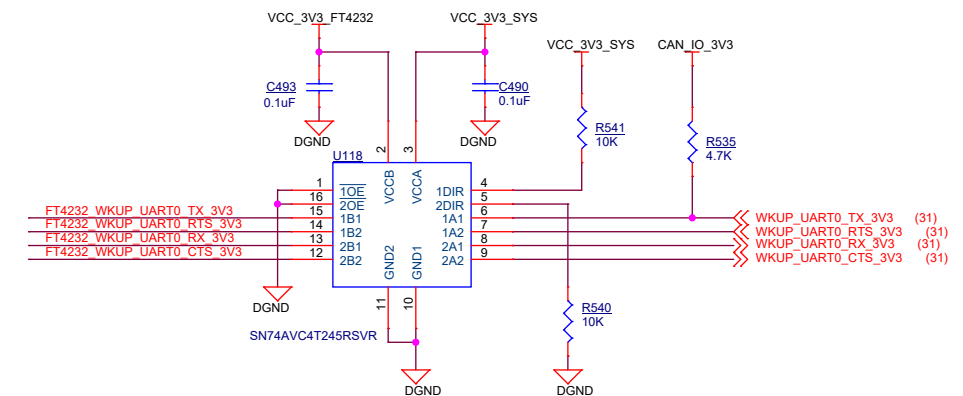
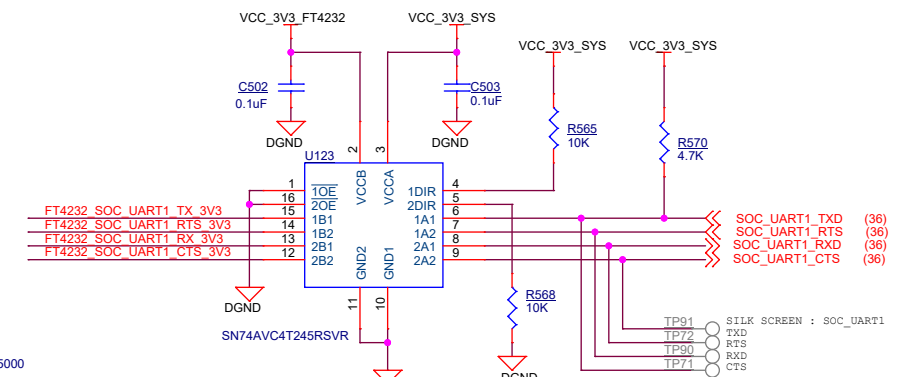
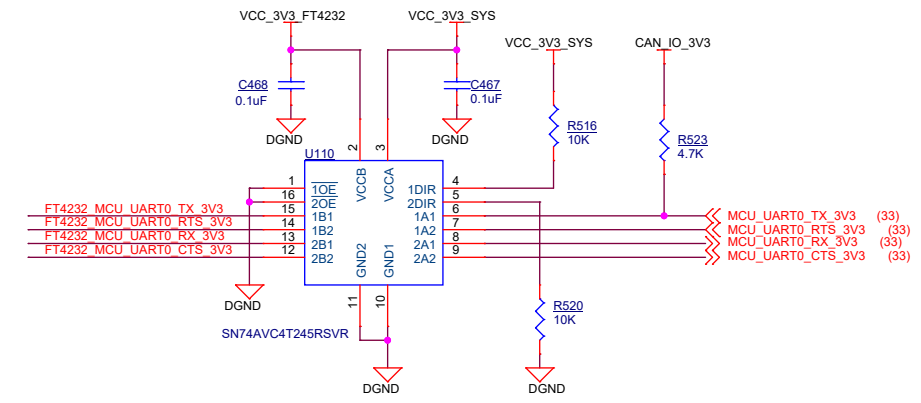
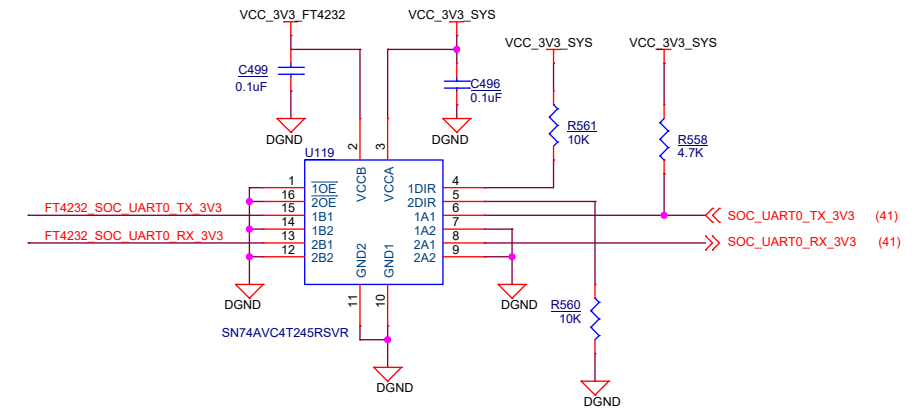
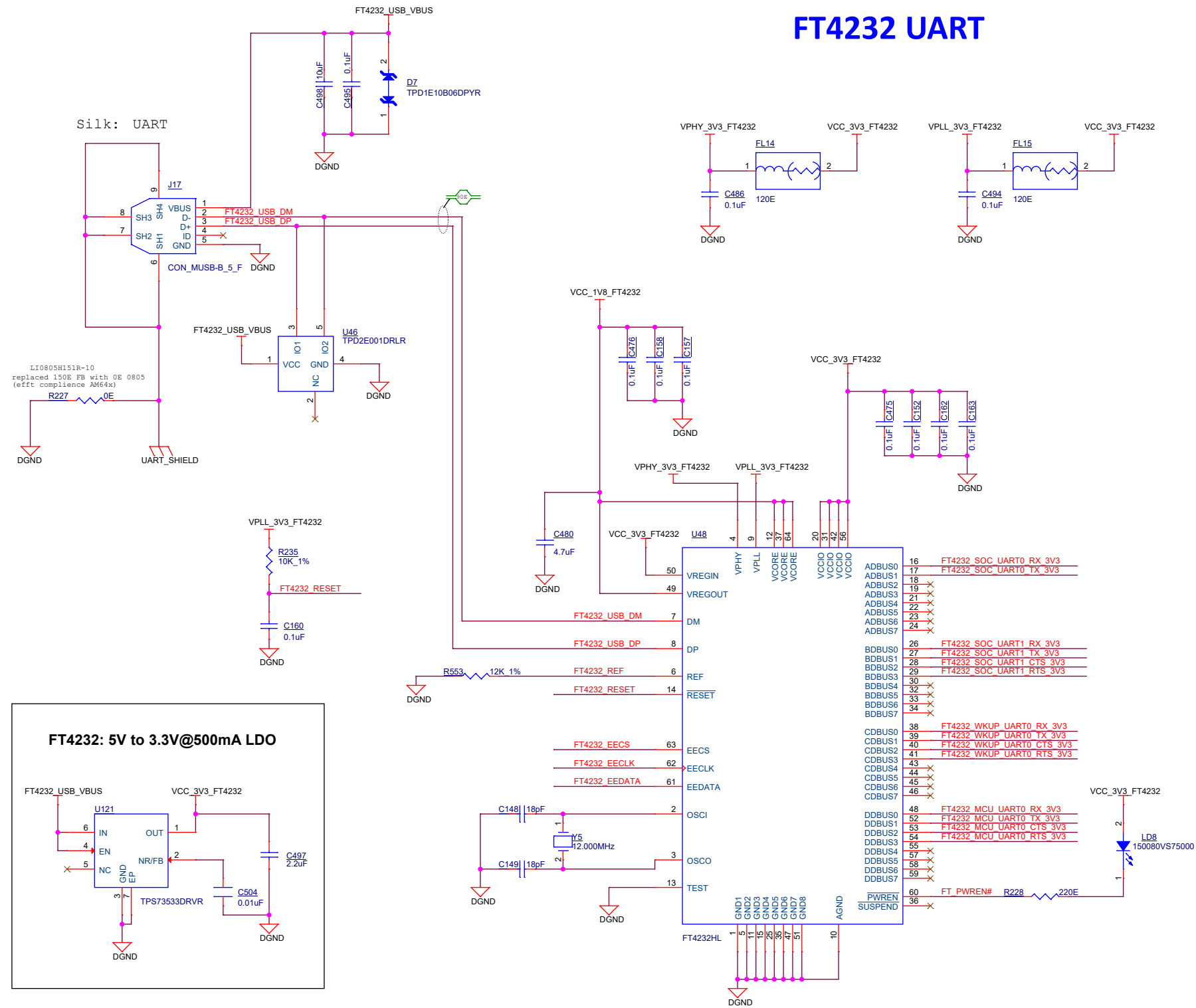
CAD NOTE: Buffers U114 and U122 need to be placed closer to the cTI-20pin connector J19 to reduce Stub length of the JTAG signals.



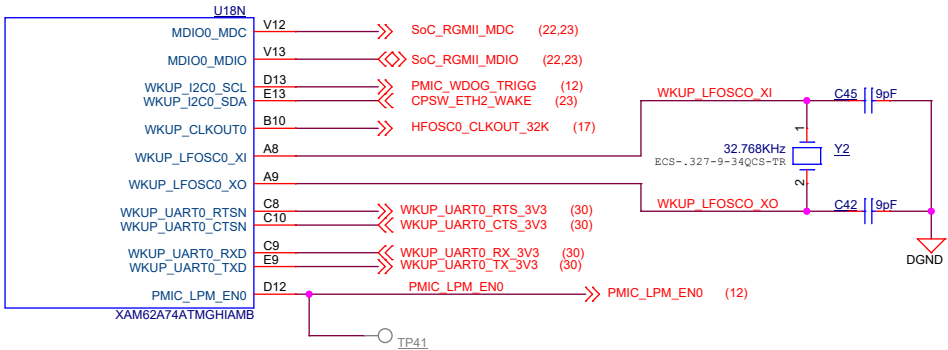
JTAG CLOCK BUFFER



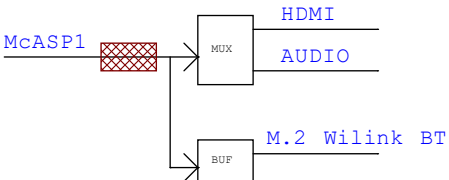
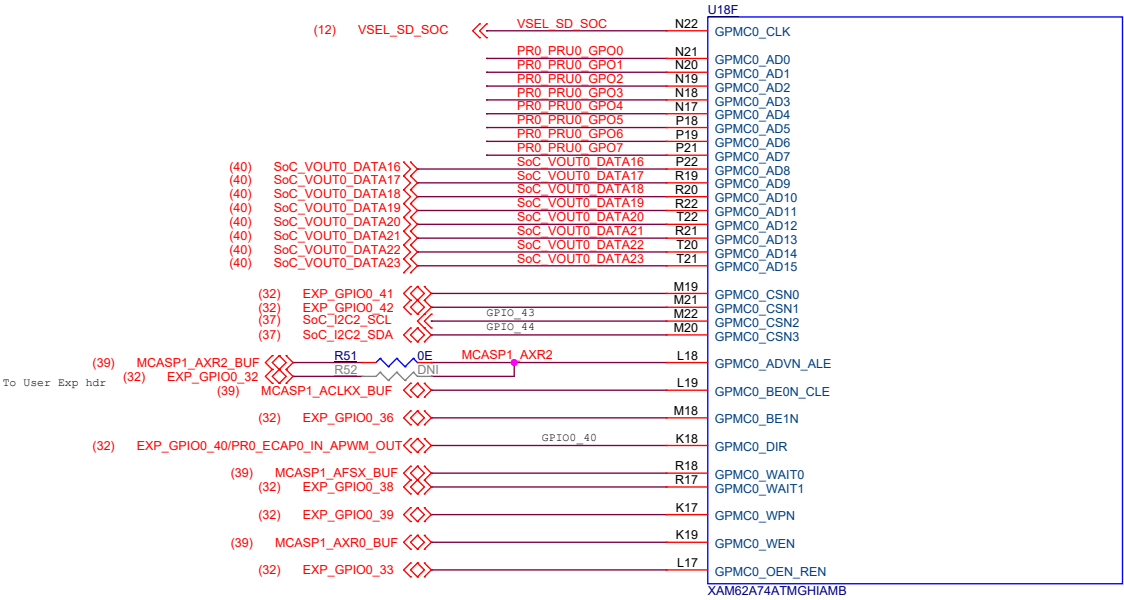
FT4232 UART



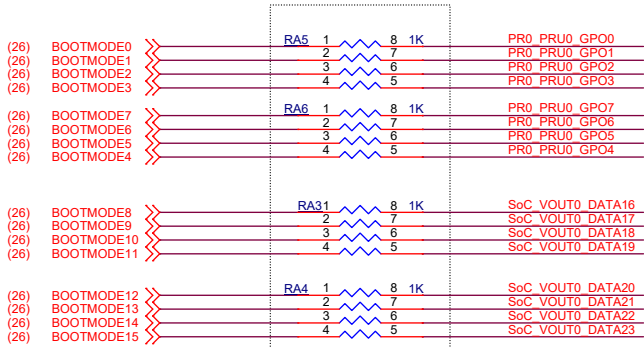
SOC WKUP DOMAIN



SOC GPMC



BOOTMODE PINS



NOTE: 1K Resistors are used to isolate the BOOTMODE control logic after the value is latched

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Title SOC WKUP & GPMC

Size PROC135E2

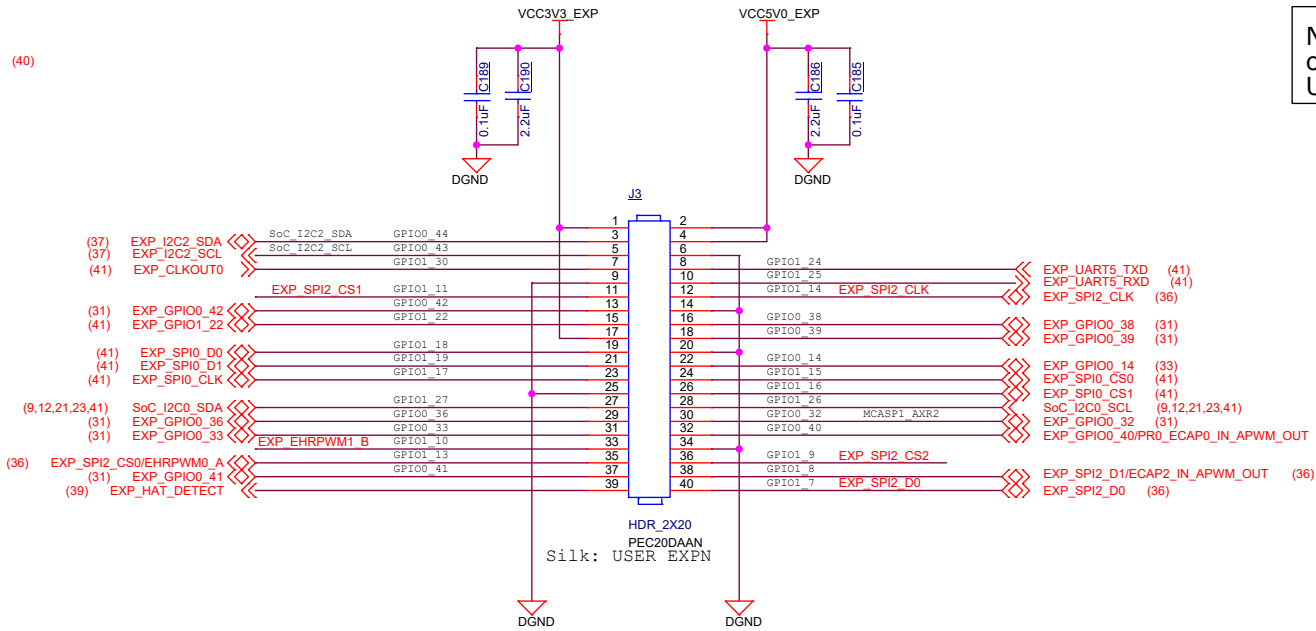
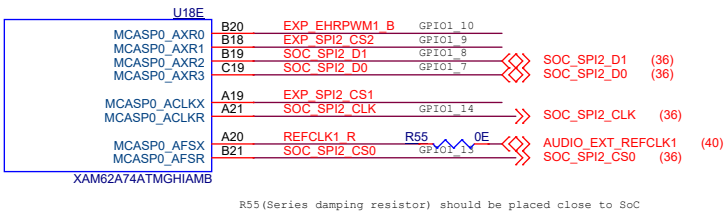
Rev

E2

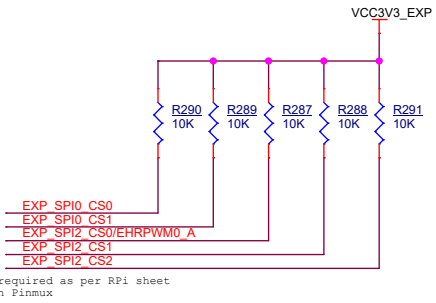
Date: Monday, September 26, 2022

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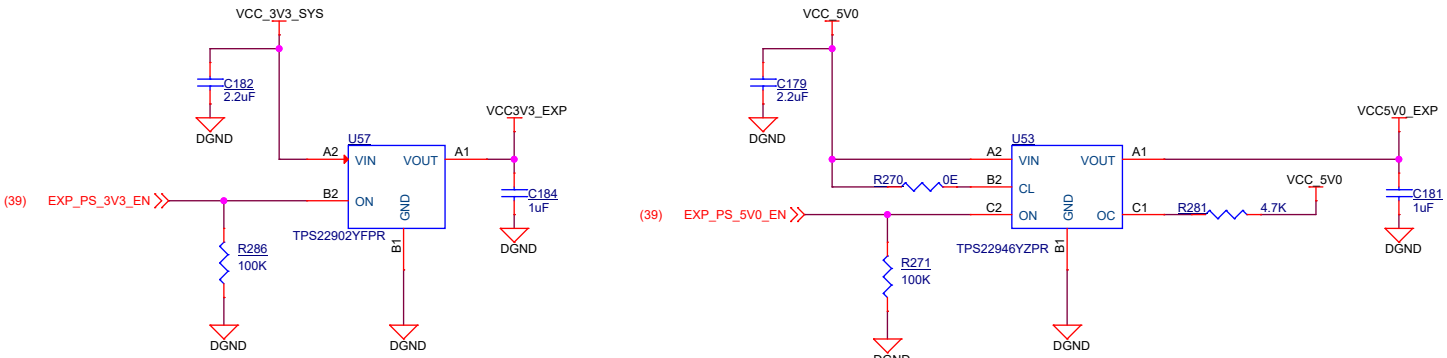
USER EXPANSION CONNECTOR



Note: Expansion boards should take care of the null modem connectivity for the UART signals (cross-over of Rx and Tx)



POWER SWITCHES FOR USER EXPANSION CONNECTOR



NOTE:

AM62A Starter Kit shall not be powered through the 5V0 or 3V3 pins on the 40-pin User Expansion Connector.

User Expansion Connector I/O are not fail-safe and shall not be driven when AM62A Starter Kit is not powered.

5V supply of User Expansion Connector is limited to sourcing 155mA max.

3V3 supply of User Expansion Connector is limited to sourcing 500mA max.

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Title USER EXPANSION CONNECTOR

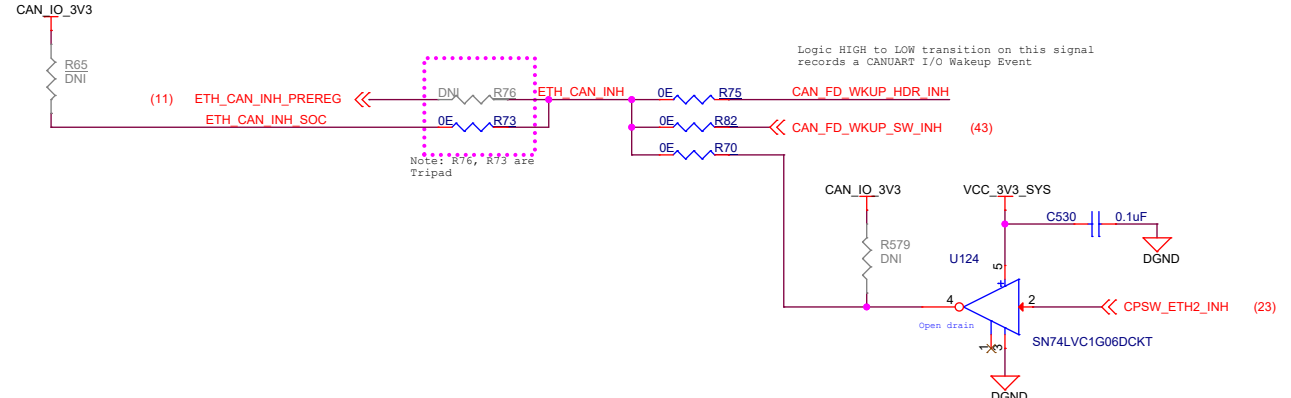
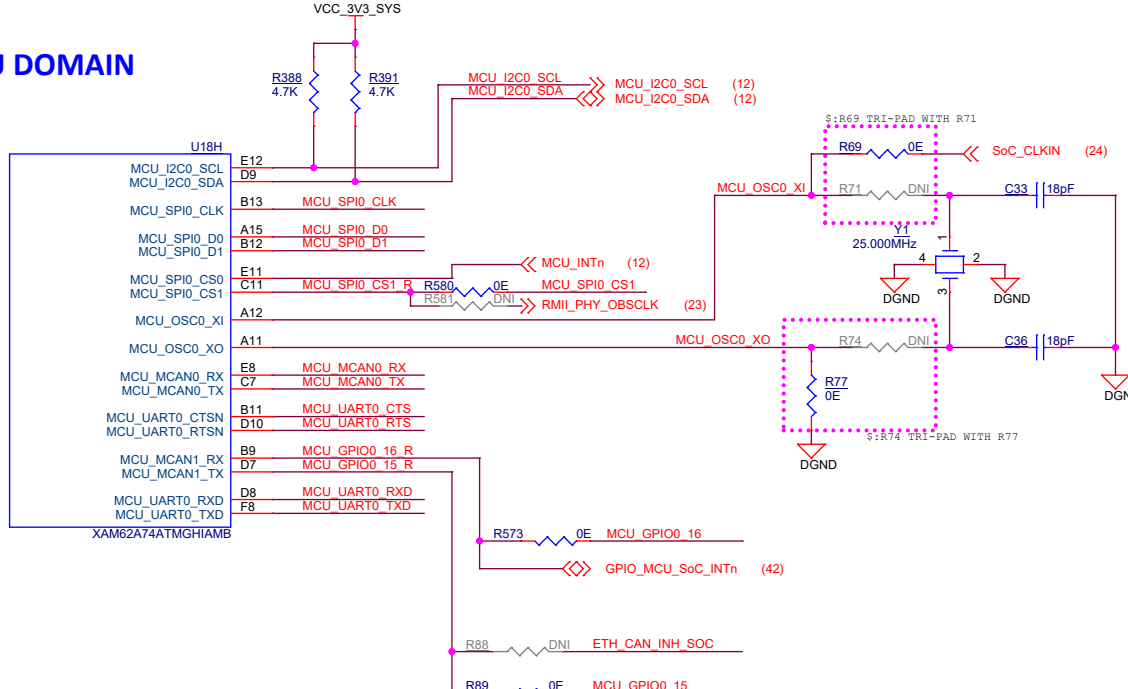
Size PROC135E2

Rev

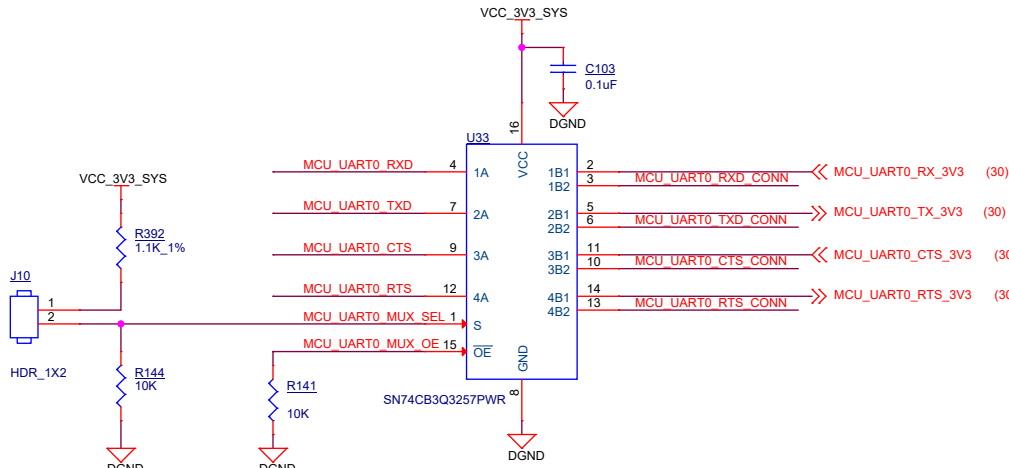
Date: Monday, September 26, 2022

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SOC - MCU DOMAIN

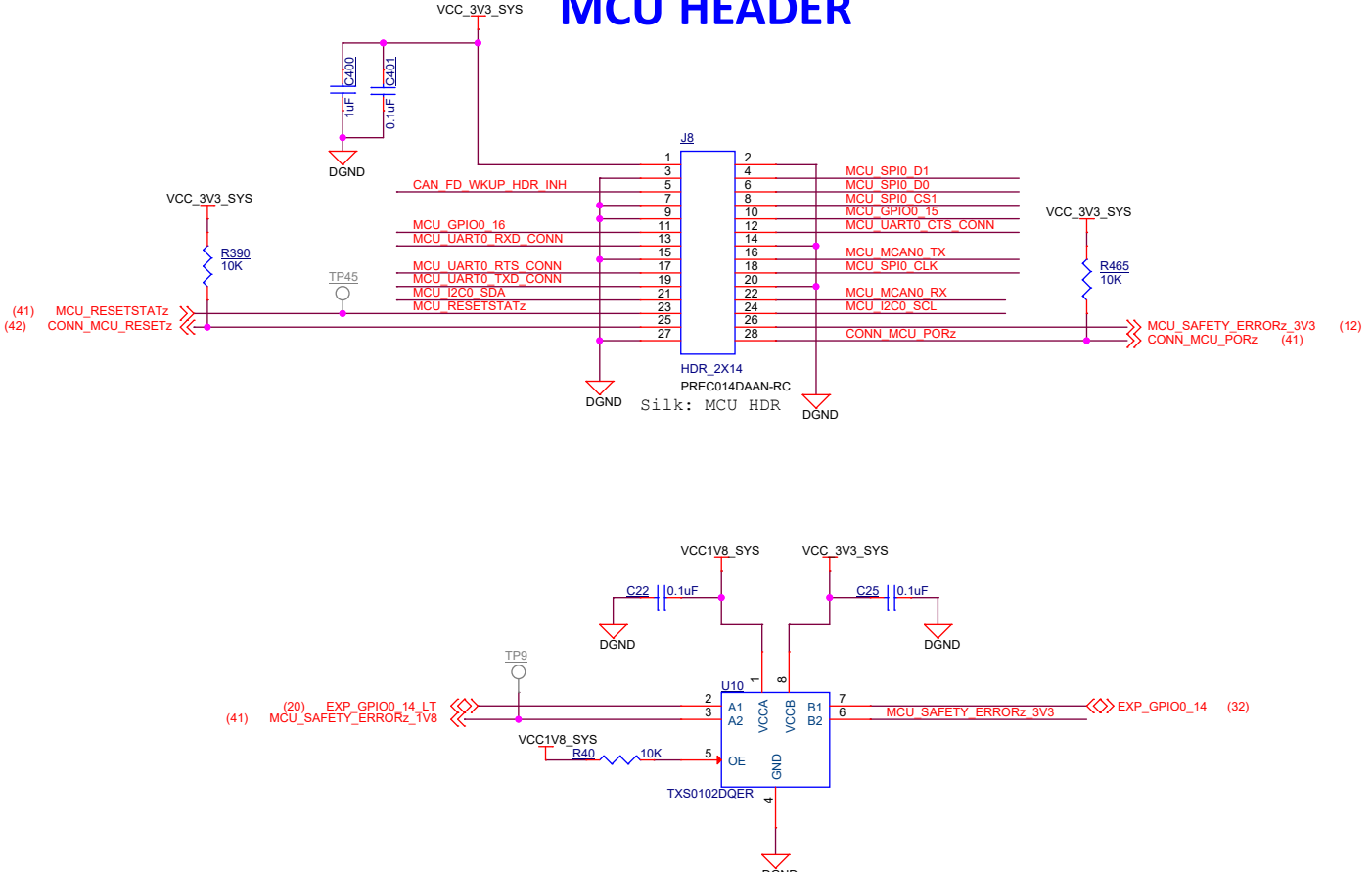


MCU UART0 MUX

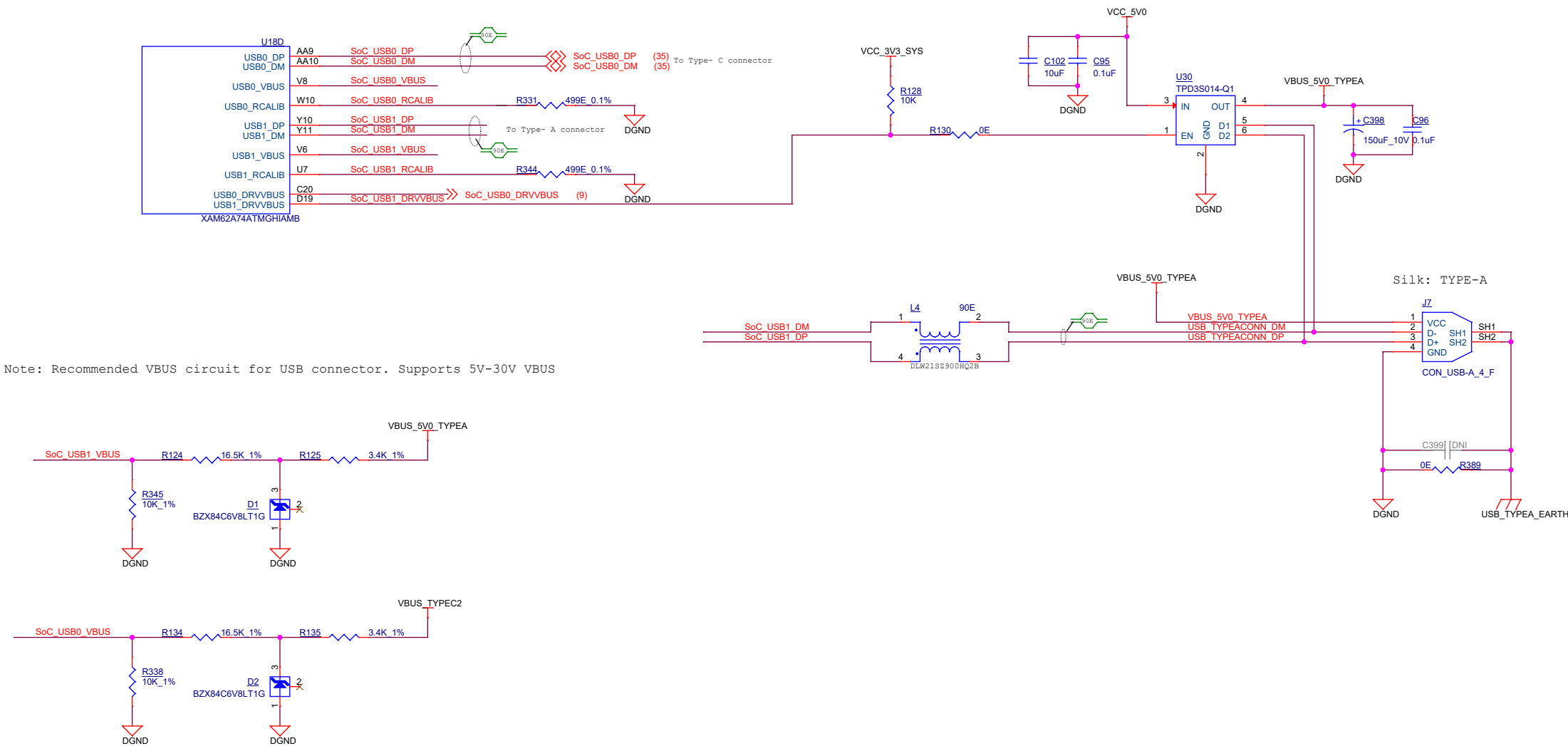


OEn	SEL	INPUT/OUTPUT An	
L	L (DEFAULT)	An=nB1	SOC - FT4232
L	H	An=nB2	SOC - MCU HEADER

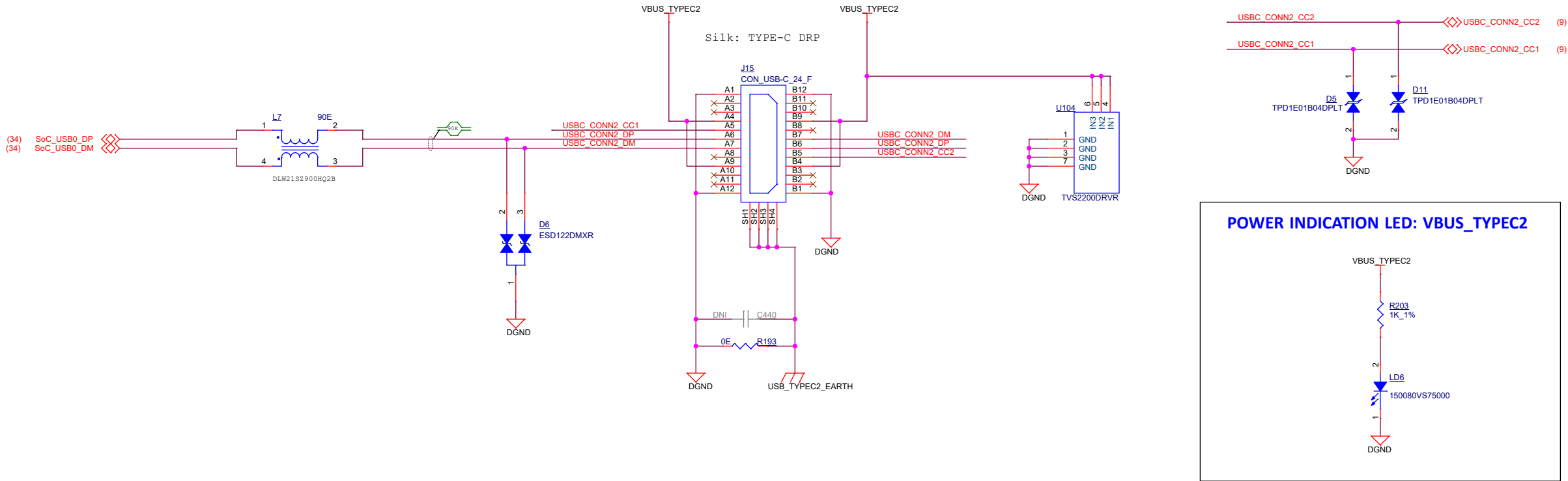
MCI HEADER



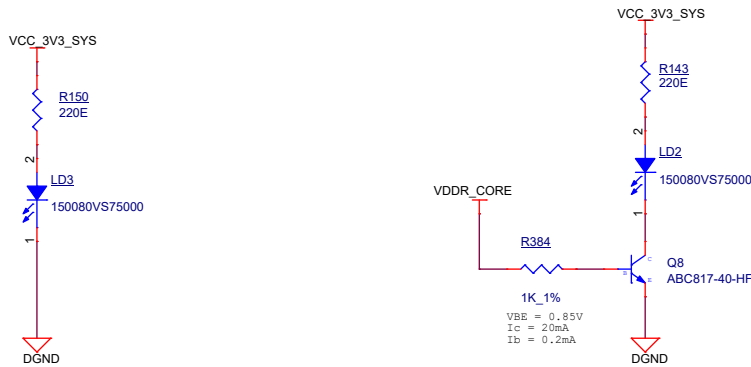
USB1 TYPE-A



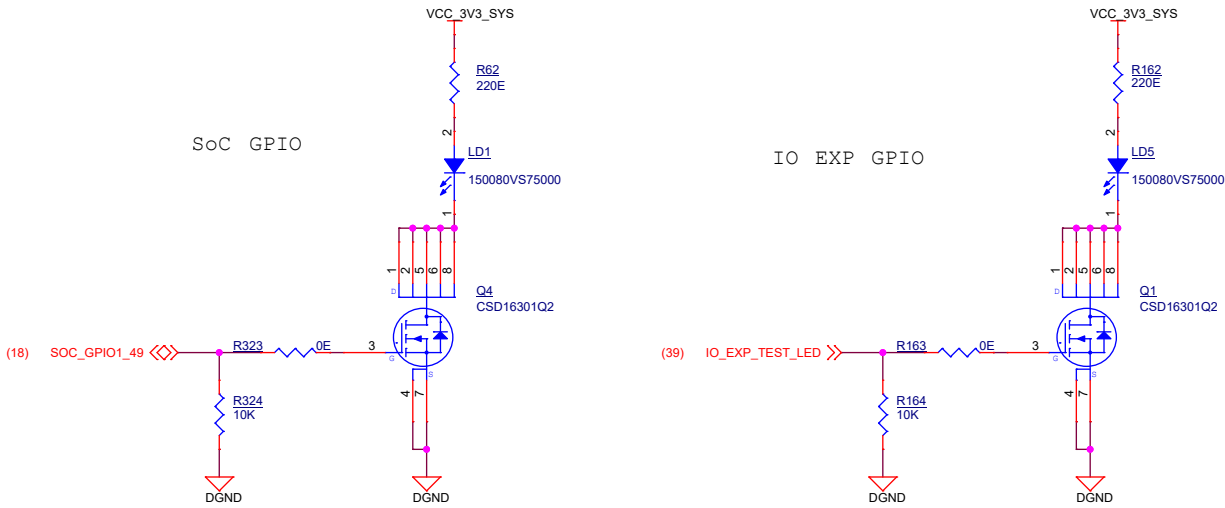
USB0 TYPE-C DRP



POWER RAIL LEDS



USER TEST LEDS



Designed for TI by Mistral Solutions Pvt Ltd



Title USB0 TYPE-C DRP & USER TEST LED

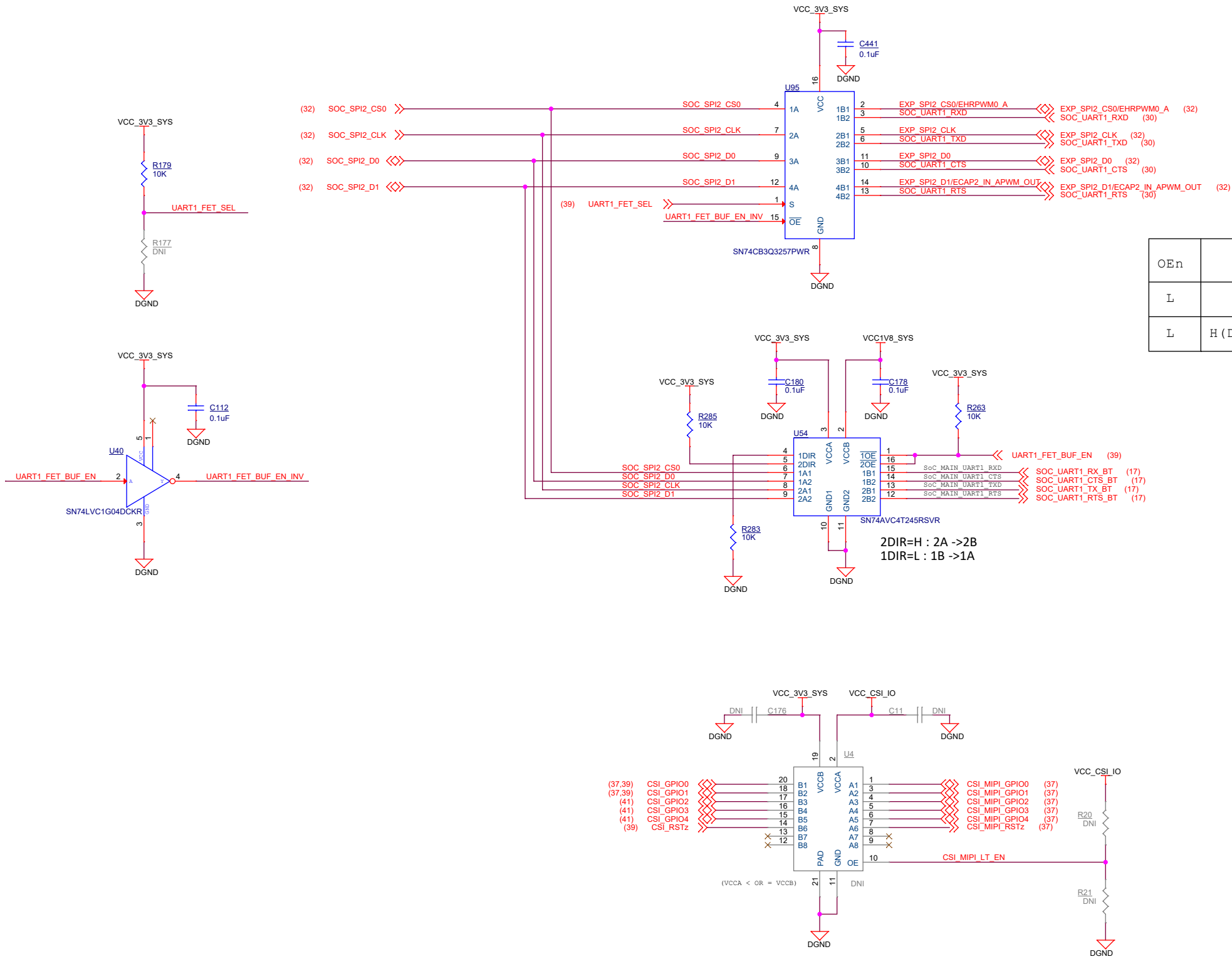
Size PROC135E2

Rev

Date: Monday, September 26, 2022

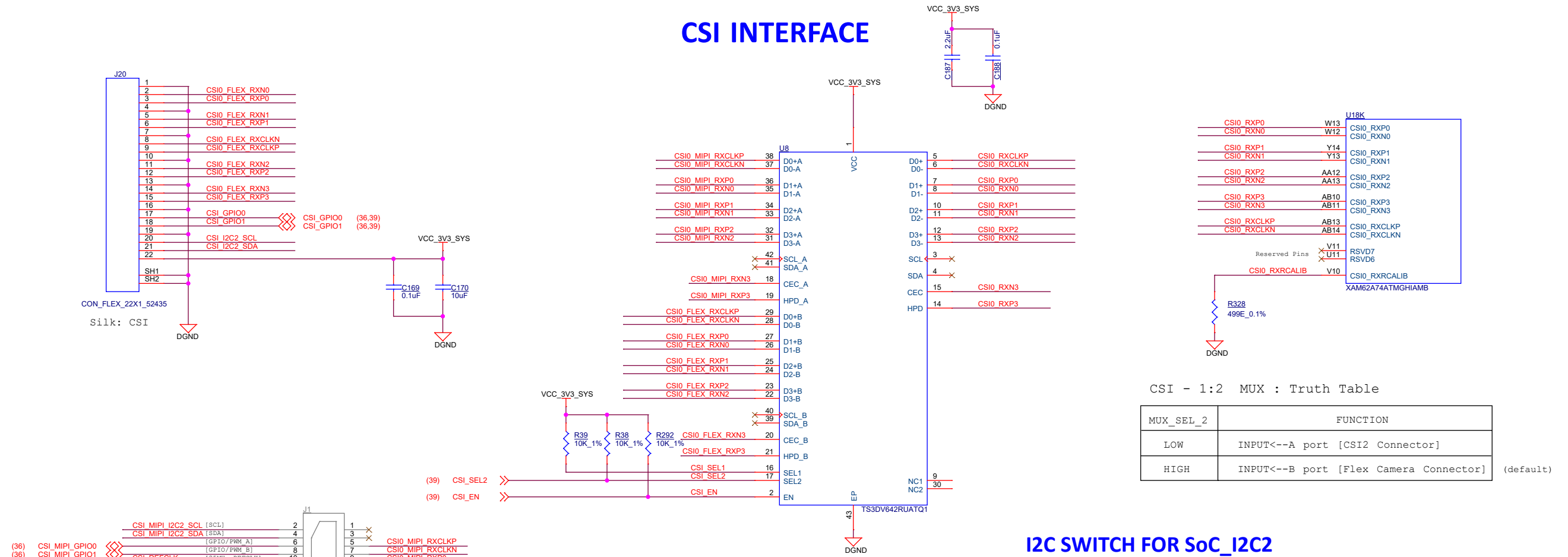
Sheet 35 of 44

SoC UART1 FET SWITCH & BUFFER

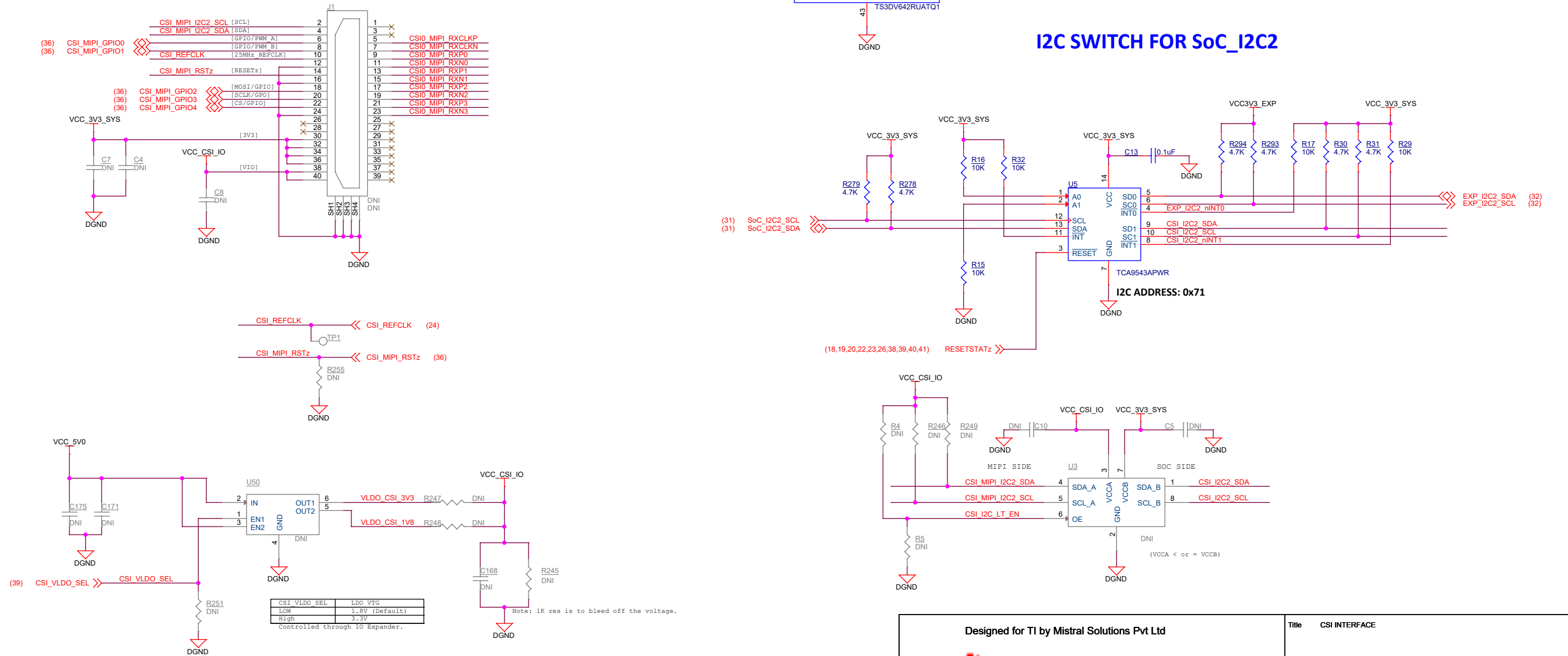


OEn	SEL	INPUT/OUTPUT	
		An	
L	L	An=nB1	SOC - EXP CONN
L	H (DEFAULT)	An=nB2	SOC - FT4232

CSI INTERFACE



I2C SWITCH FOR SoC_I2C2



Designed for TI by Mistral Solutions Pvt Ltd



Title	CSI INTERFACE
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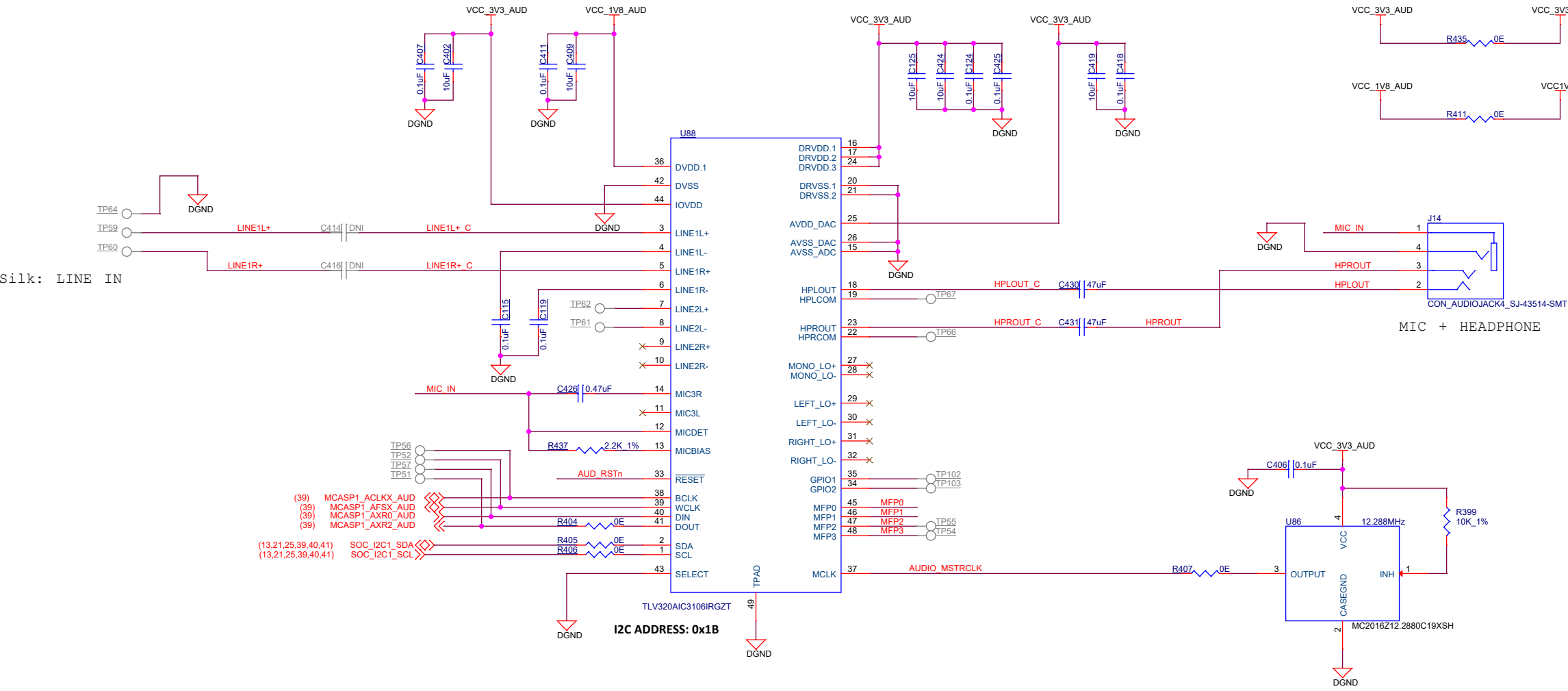
Size	PROC135E2

Date: Monday, September 26, 2022

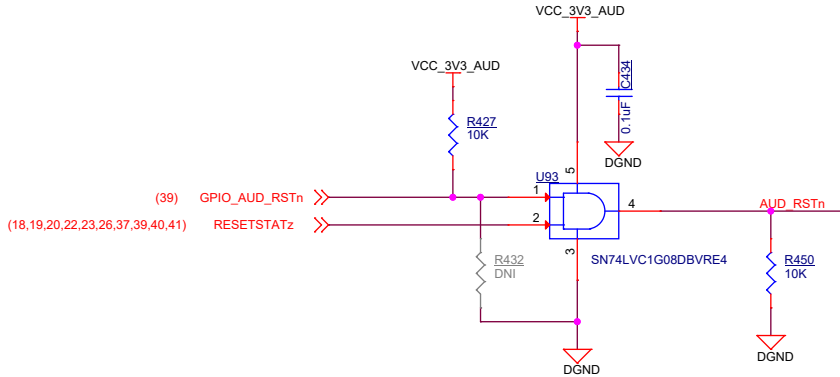
Sheet 37 of 44

Rev
55

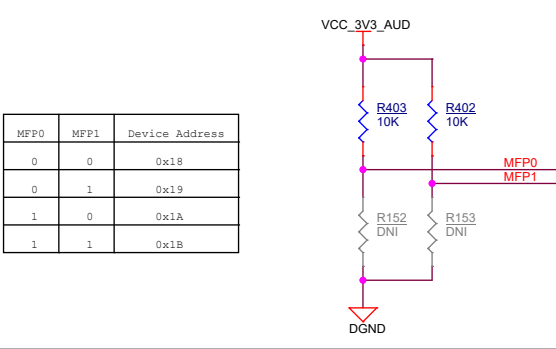
AUDIO CODEC



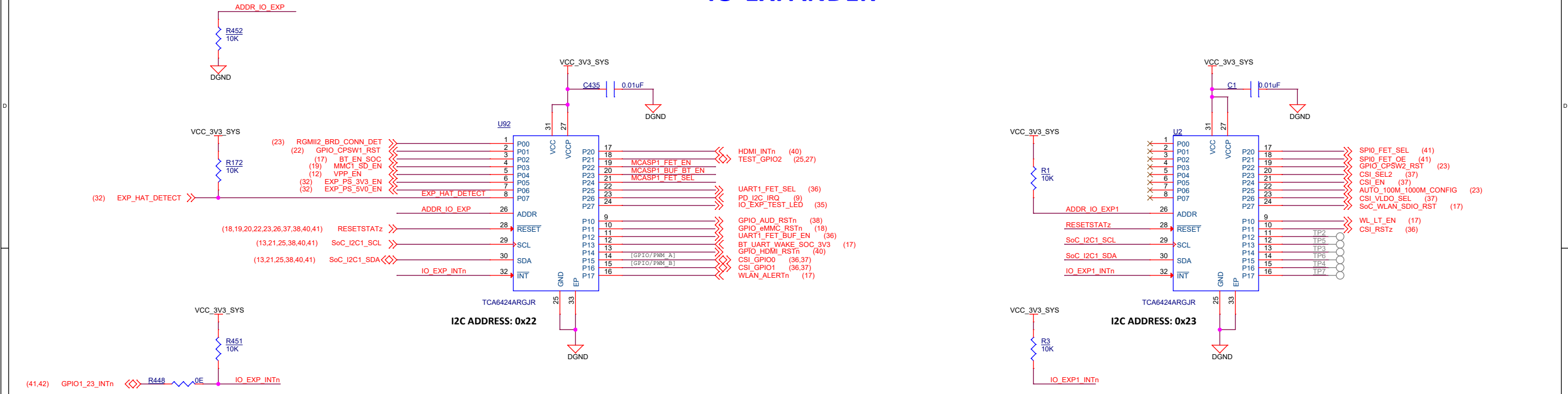
AUDIO CODEC RESET



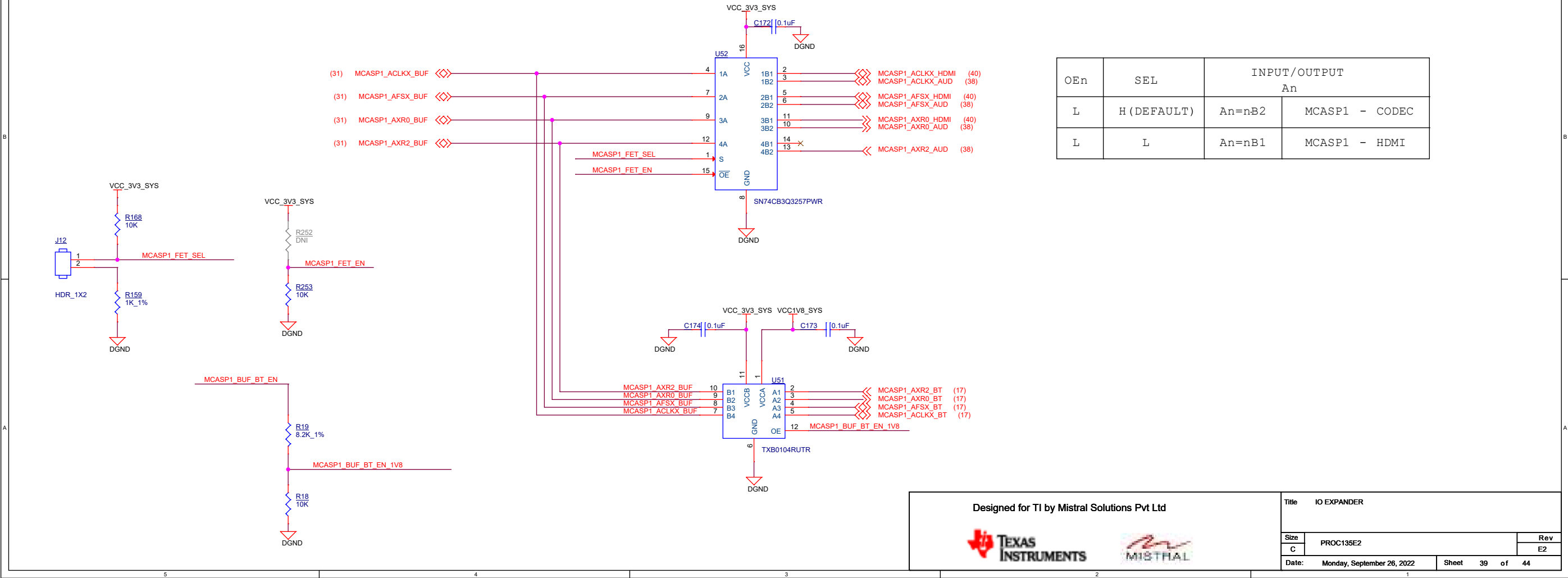
CODEC I2C ADDRESS SELECTION



IO EXPANDER

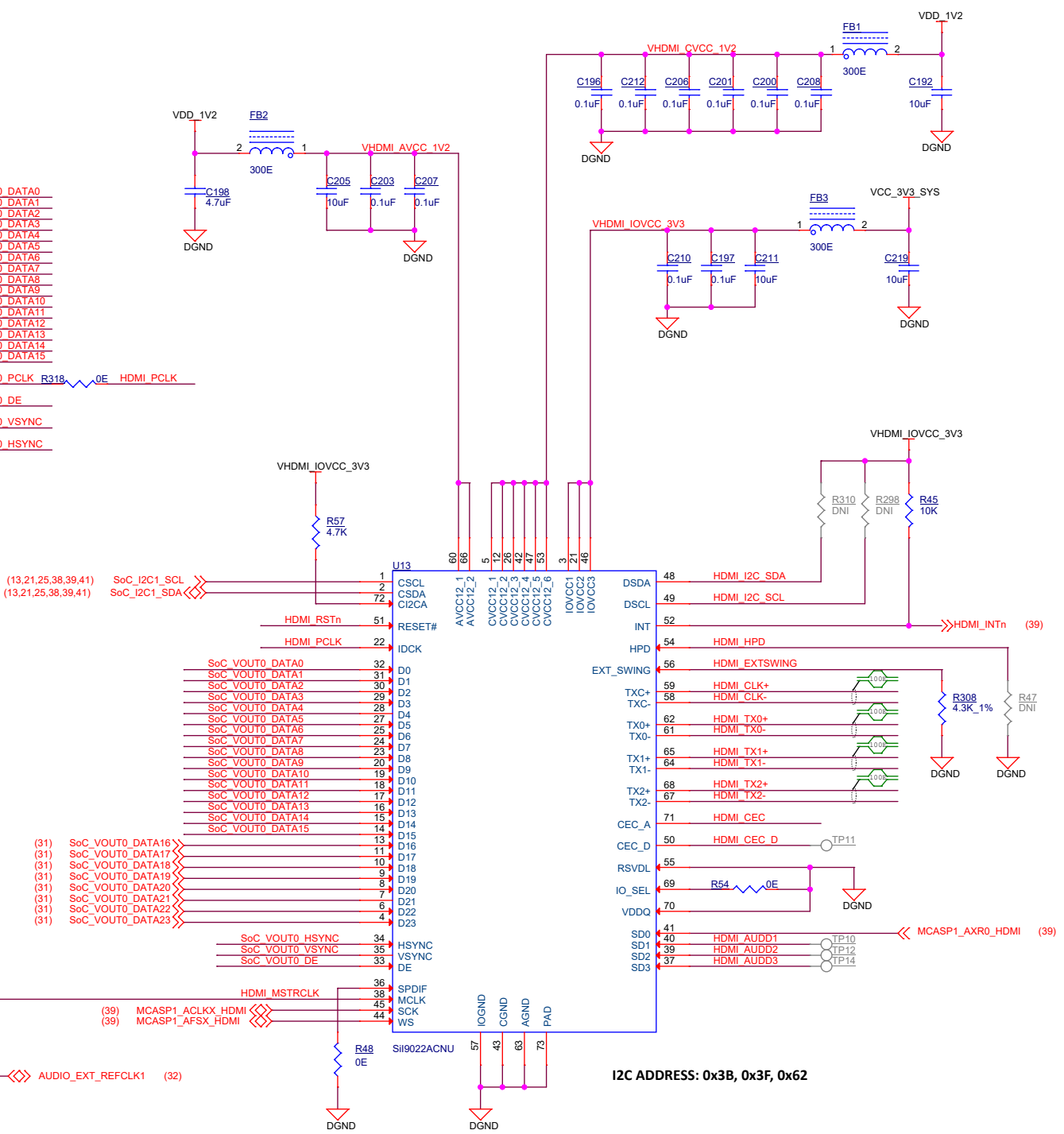
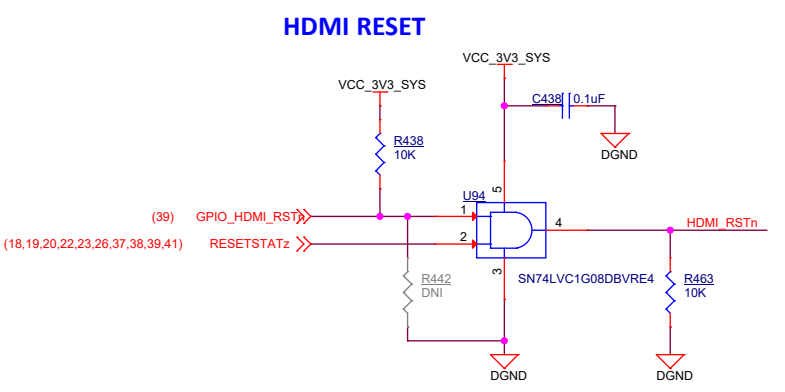
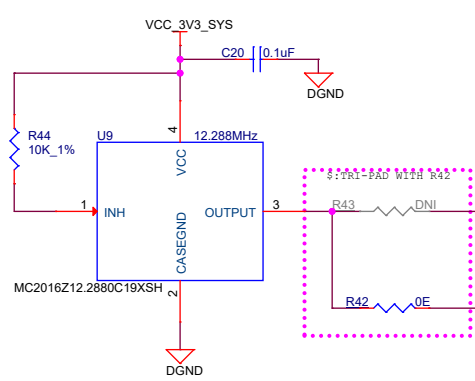


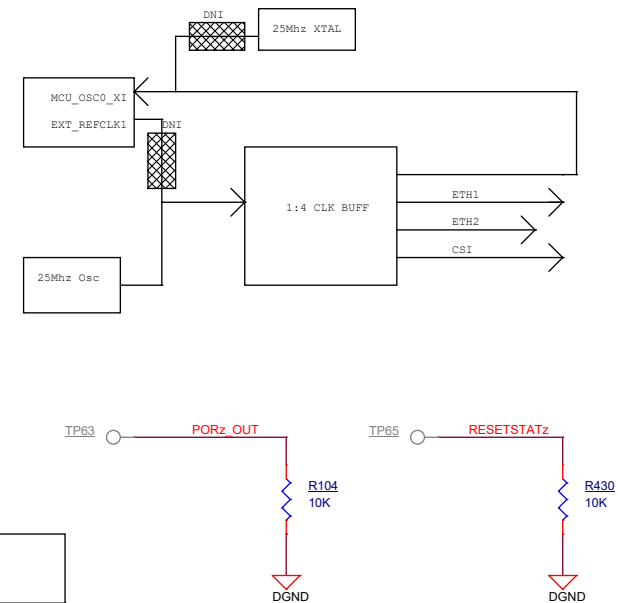
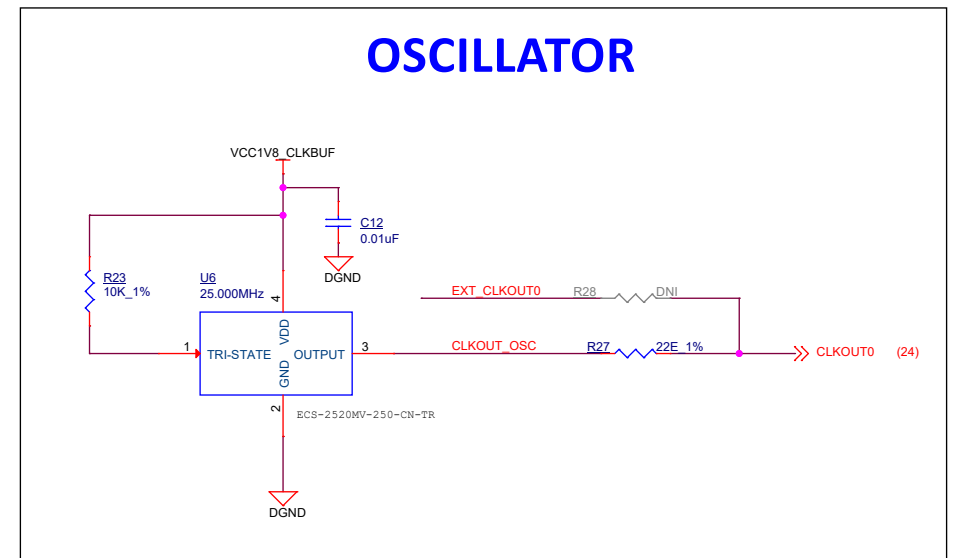
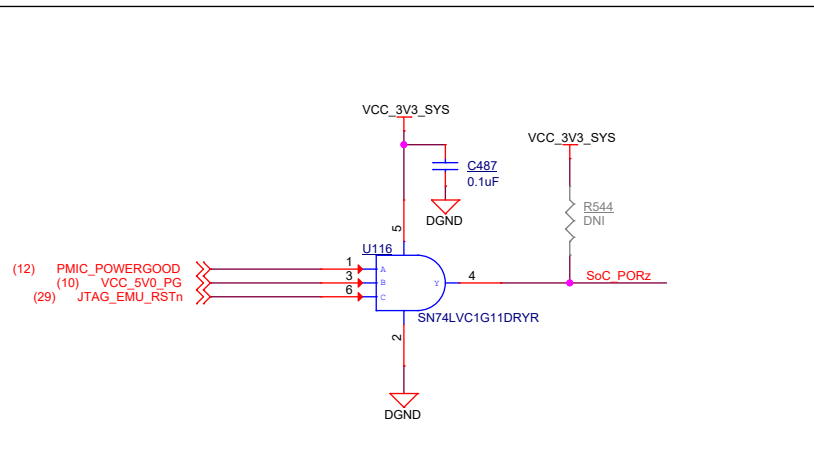
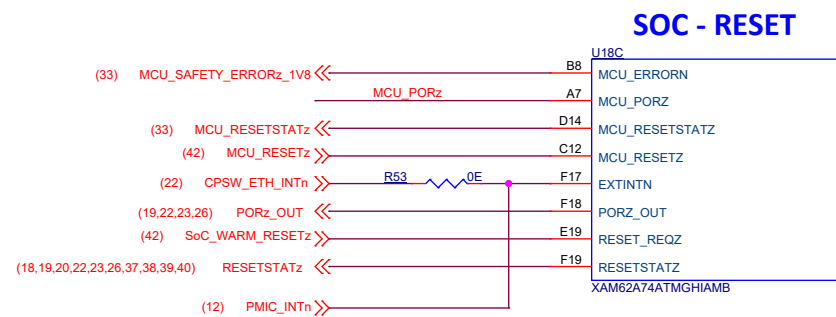
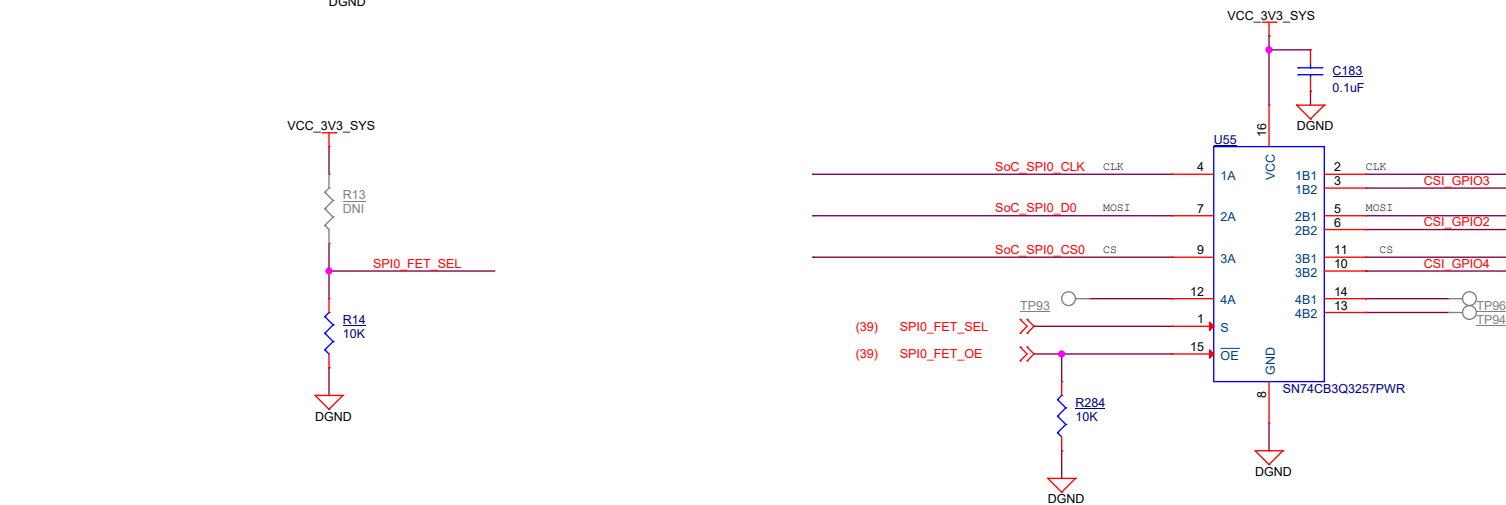
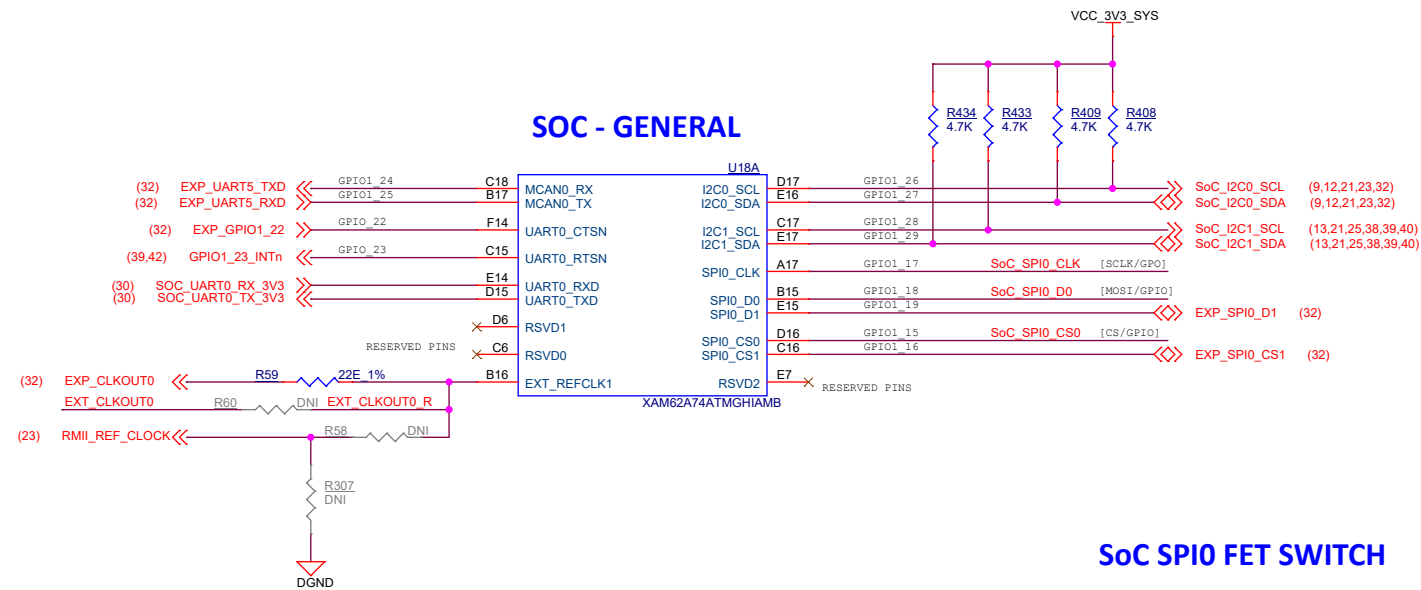
McASP1 FET SWITCH & BUFFER



HDMI INTERFACE

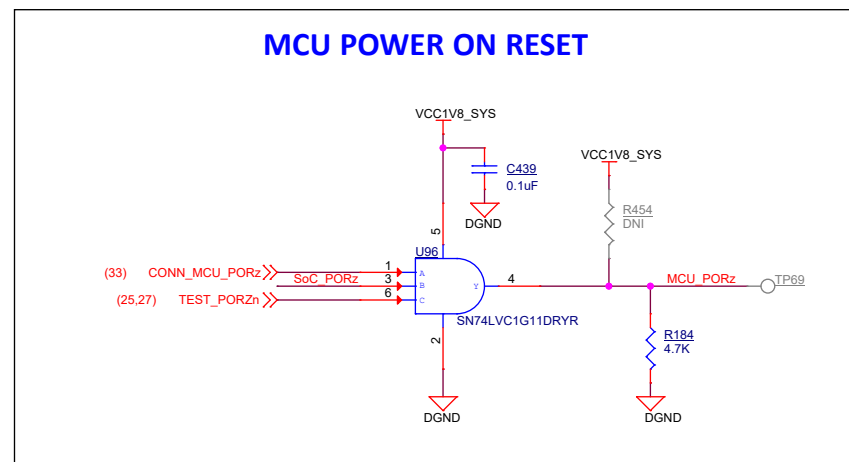
U18M	U22	SoC_VOUT0_DATA0
VOUT0_DATA0	U21	SoC_VOUT0_DATA1
VOUT0_DATA1	U20	SoC_VOUT0_DATA2
VOUT0_DATA2	U19	SoC_VOUT0_DATA3
VOUT0_DATA3	U18	SoC_VOUT0_DATA4
VOUT0_DATA4	U17	SoC_VOUT0_DATA5
VOUT0_DATA5	U16	SoC_VOUT0_DATA6
VOUT0_DATA6	U15	SoC_VOUT0_DATA7
VOUT0_DATA7	U14	SoC_VOUT0_DATA8
VOUT0_DATA8	U13	SoC_VOUT0_DATA9
VOUT0_DATA9	U12	SoC_VOUT0_DATA10
VOUT0_DATA10	U11	SoC_VOUT0_DATA11
VOUT0_DATA11	U10	SoC_VOUT0_DATA12
VOUT0_DATA12	U9	SoC_VOUT0_DATA13
VOUT0_DATA13	U8	SoC_VOUT0_DATA14
VOUT0_DATA14	U7	SoC_VOUT0_DATA15
VOUT0_DATA15		
VOUT0_PCLK	AA22	SoC_VOUT0_PCLK
VOUT0_DE	U17	SoC_VOUT0_DE
VOUT0_VSYNC	V17	SoC_VOUT0_VSYNC
VOUT0_HSYNC	T18	SoC_VOUT0_HSYNC





OEn	SEL	INPUT/OUTPUT An	
L	L (DEFAULT)	An=nB1	EXP HDR
L	H	An=nB2	MIPI CSI

Pull-down resistor on PORz_OUT is provided to keep the signal low until the processor is released from reset during the power-up sequence



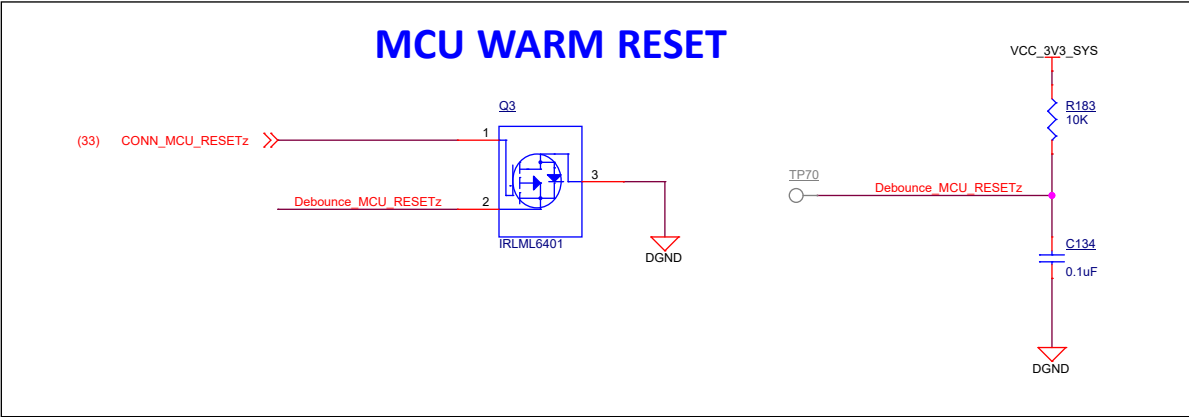
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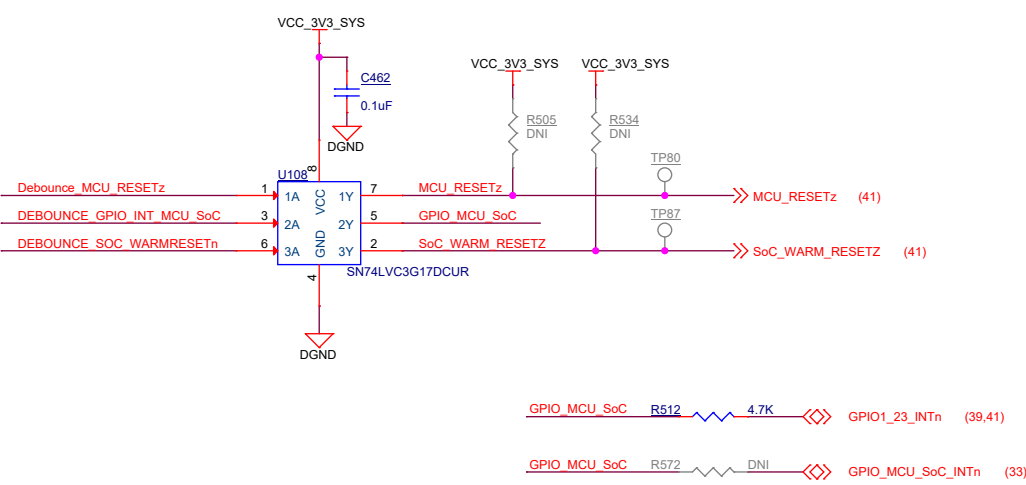
Title		OSCILLATOR	
Size	PROC135E2	Rev	
C		E2	
Date:	Monday, September 26, 2022	Sheet	41 of 44

RESET

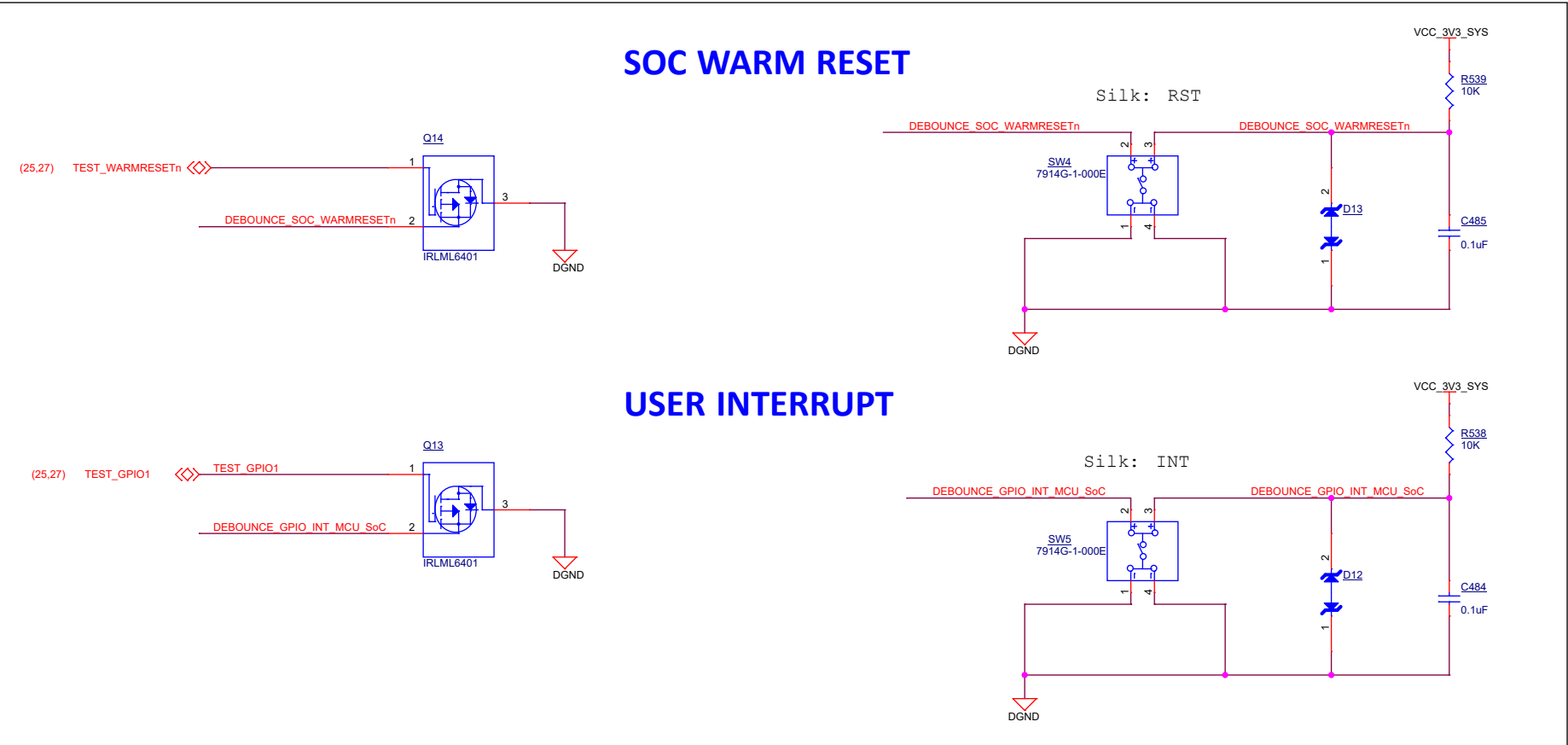
MCU WARM RESET



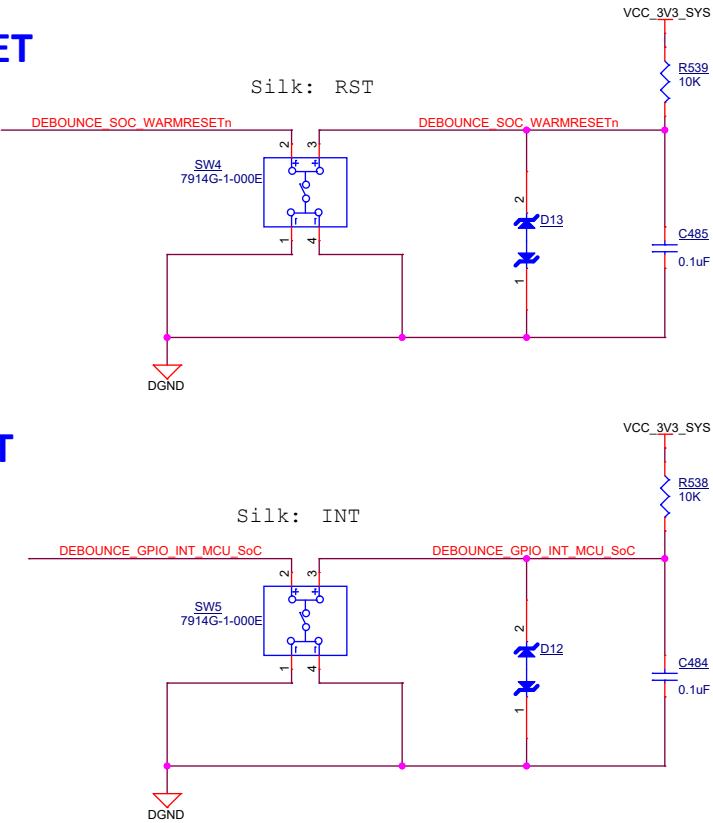
DEBOUNCE CIRCUIT



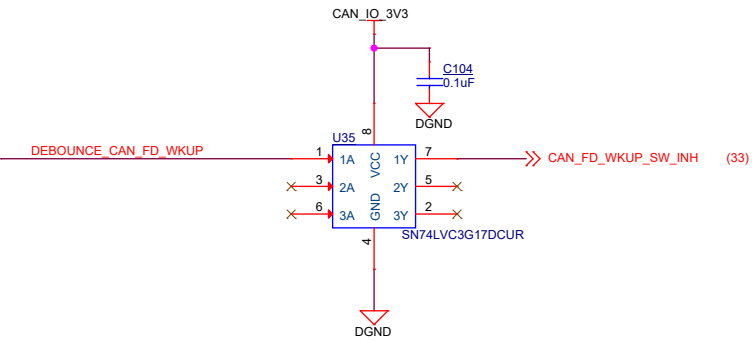
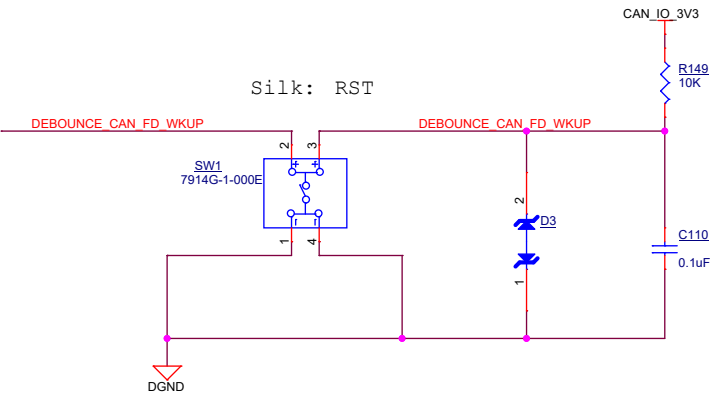
SOC WARM RESET



USER INTERRUPT



CAN-FD FAST WAKE UP SW



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Title CAN FD WKUP SW

Size PROC135E2

Rev

Date: Monday, September 26, 2022

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HARDWARE SCHEMATICS

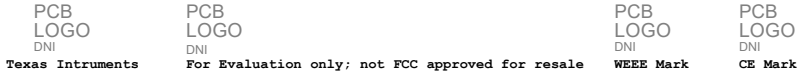
ASSEMBLY NOTES

- 1. All MSL components should be baked as per JEDEC standard.
- 2. PCB should be baked at 120 degree for 8 hours.
- 3. Board assembly must comply with workmanship standards. IPC-A-610 Class 2, unless otherwise specified.
- 4. These assemblies are ESD sensitive, ESD precautions shall be observed.
- 5. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
- 6. Provide serial numbers to the assembled boards for identification.
- 7. The assembled board are wrapped in ESD Covers(individual) and packed securely before shipment.

BARE PCB



LOGOs



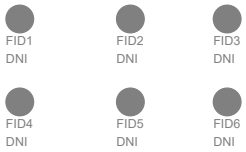
JUMPERS



AM62A SOCKET



FIDUCIALS



LABELS

Board Serial No. Assembly Revision



SCREW & WASHER FOR PCIe M.2

